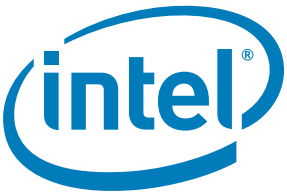

Intel® Pentium® Dual-Core Processor E5000$^{\Delta}$ Series

Datasheet

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Intel® Pentium® Dual-Core Processor E5000 Series Features

- Available at 2.66 GHz, 2.50 GHz
- Enhanced Intel Speedstep® Technology
- Supports Intel® 64Φ architecture
- Supports Execute Disable Bit capability
- FSB frequency at 800 MHz
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Advance Dynamic Execution
- Very deep out-of-order execution
- Enhanced branch prediction
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- Intel® Advanced Smart Cache
- 2 MB Level 2 cache
- Intel® Advanced Digital Media Boost
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
- System Management mode
- Multiple low-power states
- 8-way cache associativity provides improved cache hit rate on load/store operations
- 775-land Package

The Intel® Pentium® dual-core processor E5000 series is based on the Enhanced Intel® Core™ microarchitecture. The Enhanced Intel® Core™ microarchitecture combines the performance across applications and usages where end-users can truly appreciate and experience the performance. These applications include Internet audio and streaming video, image processing, video content creation, speech, 3D, CAD, games, multimedia, and multitasking user environments.

Intel® 64Φ architecture enables the processor to execute operating systems and applications written to take advantage of the Intel 64 architecture. The processor, supporting Enhanced Intel Speedstep® technology, allows tradeoffs to be made between performance and power consumption.

The Intel Pentium® dual-core processor E5000 series also includes the Execute Disable Bit capability. This feature, combined with a supported operating system, allows memory to be marked as executable or non-executable.

Revision History

Revision Number	Description	Revision Date
-001	• Initial release	August 2008
-002	• Intel® Pentium® dual-core processor E5300	December 2008

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1 Introduction

The Intel® Pentium® dual-core processor E5000 series is based on the Enhanced Intel® Core™ microarchitecture. The Intel Enhanced Core™ microarchitecture combines the performance of previous generation Desktop products with the power efficiencies of a low-power microarchitecture to enable smaller, quieter systems. The Intel® Pentium® dual-core processor E5000 series are 64-bit processors that maintain compatibility with IA-32 software.

Note: In this document, the Intel® Pentium® dual-core processor E5000 series may be referred to as "the processor."

Note: In this document, unless otherwise specified, the Intel® Pentium® dual-core processor E5000 series refers to the Intel® Pentium® dual-core processor E5200 and E5300.

The processors use Flip-Chip Land Grid Array (FC-LGA8) package technology, and plugs into a 775-land surface mount, Land Grid Array (LGA) socket, referred to as the LGA775 socket.

The processor is based on 45 nm process technology. The processors feature the Intel® Advanced Smart Cache, a shared multi-core optimized cache that significantly reduces latency to frequently used data. The processor features an 800 MHz front side bus (FSB) and 2 MB of L2 cache. The processor supports all the existing Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3), and Supplemental Streaming SIMD Extension 3 (SSSE3). The processor supports several Advanced Technologies: Execute Disable Bit, Intel® 64 architecture, and Enhanced Intel SpeedStep® Technology.

The processor's front side bus (FSB) use a split-transaction, deferred reply protocol. The FSB uses Source-Synchronous Transfer of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a "double-clocked" or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 8.5 GB/s.

Intel has enabled support components for the processor including heatsink, heatsink retention mechanism, and socket. Manufacturability is a high priority; hence, mechanical assembly may be completed from the top of the baseboard and should not require any special tooling.

1.1 Terminology

A ‘#’ symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the ‘#’ symbol implies that the signal is inverted. For example, D[3:0] = ‘HLHL’ refers to a hex ‘A’, and D[3:0]# = ‘LHLH’ also refers to a hex ‘A’ (H= High logic level, L= Low logic level).

“Front Side Bus” refers to the interface between the processor and system core logic (a.k.a. the chipset components). The FSB is a multiprocessing interface to processors, memory, and I/O.

1.1.1 Processor Terminology Definitions

Commonly used terms are explained here for clarification:

- **Intel® Pentium® dual-core processor E5000 series** — Dual core processor in the FC-LGA8 package with a 2 MB L2 cache.
- **Processor** — For this document, the term processor is the generic form of the Intel® Pentium® dual-core processor E5000 series.
- **Voltage Regulator Design Guide** — For this document “Voltage Regulator Design Guide” may be used in place of:
  - *Voltage Regulator-Down (VRD) 11.0 Processor Power Delivery Design Guidelines For Desktop LGA775 Socket*
- **Enhanced Intel® Core™ microarchitecture** — A new foundation for Intel® architecture-based desktop, mobile and mainstream server multi-core processors. For additional information refer to: http://www.intel.com/technology/architecture/coremicro/
- **Keep-out zone** — The area on or near the processor that system design can not use.
- **Processor core** — Processor die with integrated L2 cache.
- **LGA775 socket** — The processors mate with the system board through a surface mount, 775-land, LGA socket.
- **Integrated heat spreader (IHS)** —A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **Retention mechanism (RM)** — Since the LGA775 socket does not include any mechanical features for heatsink attach, a retention mechanism is required. Component thermal solutions should attach to the processor via a retention mechanism that is independent of the socket.
- **FSB (Front Side Bus)** — The electrical interface that connects the processor to the chipset. Also referred to as the processor system bus or the system bus. All memory and I/O transactions as well as interrupt messages pass between the processor and chipset over the FSB.
- **Storage conditions** — Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor lands should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to “free air”(i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
- **Functional operation** — Refers to normal operating conditions in which all processor specifications, including DC, AC, system bus, signal quality, mechanical and thermal are satisfied.
- **Execute Disable Bit** — Execute Disable Bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer over run vulnerabilities and can thus help improve the overall security of the system. See the Intel® Architecture Software Developer's Manual for more detailed information.
- **Intel® 64 Architecture**— An enhancement to Intel's IA-32 architecture, allowing the processor to execute operating systems and applications written to take advantage of the Intel 64 architecture. Further details on Intel 64 architecture and programming model can be found in the Intel Extended Memory 64 Technology

Software Developer Guide at http://developer.intel.com/technology/64bitextensions/.

- **Enhanced Intel SpeedStep® Technology** — Enhanced Intel SpeedStep Technology allows trade-offs to be made between performance and power consumptions, based on processor utilization. This may lower average power consumption (in conjunction with OS support).
- **Platform Environment Control Interface (PECI)** — A proprietary one-wire bus interface that provides a communication channel between the processor and chipset components to external monitoring devices.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1. References

Document	Location
Intel® Pentium® Dual-Core Processor E5000 Series Specification Update	http://download.intel.com/design/processor/specupdt/320467.pdf
Intel® Core™2 Duo processor E8000 and E7000 Series, and Intel® Pentium® Dual-Core Processor E5000 Series Thermal and Mechanical Design Guidelines	www.intel.com/design/processor/designex/318734.htm
Voltage Regulator-Down (VRD) 11.0 Processor Power Delivery Design Guidelines For Desktop LGA775 Socket	http://www.intel.com/design/processor/applnots/313214.htm
LGA775 Socket Mechanical Design Guide	http://intel.com/design/Pentium4/guides/302666.htm
Intel® 64 and IA-32 Intel Architecture Software Developer's Manuals Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide, Part 1 Volume 3B: System Programming Guide, Part 2	http://www.intel.com/products/processor/manuals/

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2 Electrical Specifications

This chapter describes the electrical characteristics of the processor interfaces and signals. DC electrical characteristics are provided.

2.1 Power and Ground Lands

The processor has VCC (power), VTT, and VSS (ground) inputs for on-chip power distribution. All power lands must be connected to V_{CC}, while all VSS lands must be connected to a system ground plane. The processor VCC lands must be supplied the voltage determined by the **V**oltage **ID**entification (VID) lands.

The signals denoted as VTT provide termination for the front side bus and power to the I/O buffers. A separate supply must be implemented for these lands, that meets the V_{TT} specifications outlined in Table 4.

2.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings. This may cause voltages on power planes to sag below their minimum specified values if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic or aluminum-polymer capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. The motherboard must be designed to ensure that the voltage provided to the processor remains within the specifications listed in Table 4. Failure to do so can result in timing violations or reduced lifetime of the component.

2.2.1 V_{CC} Decoupling

V_{CC} regulator solutions need to provide sufficient decoupling capacitance to satisfy the processor voltage specifications. This includes bulk capacitance with low effective series resistance (ESR) to keep the voltage rail within specifications during large swings in load current. In addition, ceramic decoupling capacitors are required to filter high frequency content generated by the front side bus and processor activity. Consult the *Voltage Regulator-Down (VRD) 11.0 Processor Power Delivery Design Guidelines For Desktop LGA775 Socket* for further information. Contact your Intel field representative for additional information.

2.2.2 V_{TT} Decoupling

Decoupling must be provided on the motherboard. Decoupling solutions must be sized to meet the expected load. To ensure compliance with the specifications, various factors associated with the power delivery solution must be considered including regulator type, power plane and trace sizing, and component placement. A conservative decoupling solution would consist of a combination of low ESR bulk capacitors and high frequency ceramic capacitors.

2.2.3 FSB Decoupling

The processor integrates signal termination on the die. In addition, some of the high frequency capacitance required for the FSB is included on the processor package. However, additional high frequency capacitance must be added to the motherboard to properly decouple the return currents from the front side bus. Bulk decoupling must also be provided by the motherboard for proper [A]GTL+ bus operation.

2.3 Voltage Identification

The Voltage Identification (VID) specification for the processor is defined by the *Voltage Regulator-Down (VRD) 11.0 Processor Power Delivery Design Guidelines For Desktop LGA775 Socket*. The voltage set by the VID signals is the reference VR output voltage to be delivered to the processor VCC lands (see Chapter 2.6.3 for V_{CC} overshoot specifications). Refer to Table 12 for the DC specifications for these signals. Voltages for each processor frequency is provided in Table 4.

Note: To support the Deeper Sleep State the platform must use a VRD 11.1 compliant solution. The Deeper Sleep State also requires additional platform support.

Individual processor VID values may be calibrated during manufacturing such that two devices at the same core speed may have different default VID settings. This is reflected by the VID Range values provided in Table 4. Refer to the *Intel® Pentium® dual-core Processor E5000 Series Specification Update* for further details on specific valid core frequency and VID values of the processor. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep® technology, or Extended HALT State).

The processor uses eight voltage identification signals, VID[7:0], to support automatic selection of power supply voltages. Table 2 specifies the voltage level corresponding to the state of VID[7:0]. A ‘1’ in this table refers to a high voltage level and a ‘0’ refers to a low voltage level. If the processor socket is empty (VID[7:0] = 11111110), or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself.

The processor provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage (V_{CC}). This will represent a DC shift in the load line. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target core voltage. Transitions above the specified VID are not permitted. Table 4 includes VID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 5, and Figure 1, as measured across the VCC_SENSE and VSS_SENSE lands.

The VRM or VRD utilized must be capable of regulating its output to the value defined by the new VID. DC specifications for dynamic VID transitions are included in Table 4 and Table 5 . Refer to the Voltage Regulator Design Guide for further details.

Table 2. Voltage Identification Definition

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Voltage
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	1	0	1.6
0	0	0	0	0	1	0	0	1.5875
0	0	0	0	0	1	1	0	1.575
0	0	0	0	1	0	0	0	1.5625
0	0	0	0	1	0	1	0	1.55
0	0	0	0	1	1	0	0	1.5375
0	0	0	0	1	1	1	0	1.525
0	0	0	1	0	0	0	0	1.5125
0	0	0	1	0	0	1	0	1.5
0	0	0	1	0	1	0	0	1.4875
0	0	0	1	0	1	1	0	1.475
0	0	0	1	1	0	0	0	1.4625
0	0	0	1	1	0	1	0	1.45
0	0	0	1	1	1	0	0	1.4375
0	0	0	1	1	1	1	0	1.425
0	0	1	0	0	0	0	0	1.4125
0	0	1	0	0	0	1	0	1.4
0	0	1	0	0	1	0	0	1.3875
0	0	1	0	0	1	1	0	1.375
0	0	1	0	1	0	0	0	1.3625
0	0	1	0	1	0	1	0	1.35
0	0	1	0	1	1	0	0	1.3375
0	0	1	0	1	1	1	0	1.325
0	0	1	1	0	0	0	0	1.3125
0	0	1	1	0	0	1	0	1.3
0	0	1	1	0	1	0	0	1.2875
0	0	1	1	0	1	1	0	1.275
0	0	1	1	1	0	0	0	1.2625
0	0	1	1	1	0	1	0	1.25
0	0	1	1	1	1	0	0	1.2375
0	0	1	1	1	1	1	0	1.225
0	1	0	0	0	0	0	0	1.2125
0	1	0	0	0	0	1	0	1.2
0	1	0	0	0	1	0	0	1.1875
0	1	0	0	0	1	1	0	1.175
0	1	0	0	1	0	0	0	1.1625
0	1	0	0	1	0	1	0	1.15
0	1	0	0	1	1	0	0	1.1375
0	1	0	0	1	1	1	0	1.125
0	1	0	1	0	0	0	0	1.1125
0	1	0	1	0	0	1	0	1.1
0	1	0	1	0	1	0	0	1.0875
0	1	0	1	0	1	1	0	1.075
0	1	0	1	1	0	0	0	1.0625
0	1	0	1	1	0	1	0	1.05
0	1	0	1	1	1	0	0	1.0375
0	1	0	1	1	1	1	0	1.025
0	1	1	0	0	0	0	0	1.0125
0	1	1	0	0	0	1	0	1
0	1	1	0	0	1	0	0	0.9875
0	1	1	0	0	1	1	0	0.975
0	1	1	0	1	0	0	0	0.9625
0	1	1	0	1	0	1	0	0.95
0	1	1	0	1	1	0	0	0.9375
0	1	1	0	1	1	1	0	0.925
0	1	1	1	0	0	0	0	0.9125
0	1	1	1	0	0	1	0	0.9
0	1	1	1	0	1	0	0	0.8875
0	1	1	1	0	1	1	0	0.875
0	1	1	1	1	0	0	0	0.8625
0	1	1	1	1	0	1	0	0.85
0	1	1	1	1	1	0	0	0.8375
0	1	1	1	1	1	1	0	0.825
1	0	0	0	0	0	0	0	0.8125
1	0	0	0	0	0	1	0	0.8
1	0	0	0	0	1	0	0	0.7875
1	0	0	0	0	1	1	0	0.775
1	0	0	0	1	0	0	0	0.7625
1	0	0	0	1	0	1	0	0.75
1	0	0	0	1	1	0	0	0.7375
1	0	0	0	1	1	1	0	0.725
1	0	0	1	0	0	0	0	0.7125
1	0	0	1	0	0	1	0	0.7
1	0	0	1	0	1	0	0	0.6875
1	0	0	1	0	1	1	0	0.675
1	0	0	1	1	0	0	0	0.6625
1	0	0	1	1	0	1	0	0.65
1	0	0	1	1	1	0	0	0.6375
1	0	0	1	1	1	1	0	0.625
1	0	1	0	0	0	0	0	0.6125
1	0	1	0	0	0	1	0	0.6
1	0	1	0	0	1	0	0	0.5875
1	0	1	0	0	1	1	0	0.575
1	0	1	0	1	0	0	0	0.5625
1	0	1	0	1	0	1	0	0.55
1	0	1	0	1	1	0	0	0.5375
1	0	1	0	1	1	1	0	0.525
1	0	1	1	0	0	0	0	0.5125
1	0	1	1	0	0	1	0	0.5
1	1	1	1	1	1	1	0	OFF

2.4 Reserved, Unused, and TESTHI Signals

All RESERVED lands must remain unconnected. Connection of these lands to V_{CC}, V_{SS}, V_{TT}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Chapter 4 for a land listing of the processor and the location of all RESERVED lands.

In a system level design, on-die termination has been included by the processor to allow signals to be terminated within the processor silicon. Most unused GTL+ inputs should be left as no connects as GTL+ termination is provided on the processor silicon. However, see Table 7 for details on GTL+ signals that do not include on-die termination.

Unused active high inputs, should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected, however this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ± 20% of the impedance of the motherboard trace for front side bus signals. For unused GTL+ input or I/O signals, use pull-up resistors of the same value as the on-die termination resistors (R_{TT}). For details see Table 14.

TAP and CMOS signals do not include on-die termination. Inputs and utilized outputs must be terminated on the motherboard. Unused outputs may be terminated on the motherboard or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing.

All TESTHI[12,10:0] lands should be individually connected to V_{TT} via a pull-up resistor which matches the nominal trace impedance.

The TESTHI signals may use individual pull-up resistors or be grouped together as detailed below. A matched resistor must be used for each group:

- TESTHI[1:0]
- TESTHI[7:2]
- TESTHI8/FC42 – cannot be grouped with other TESTHI signals
- TESTHI9/FC43 – cannot be grouped with other TESTHI signals
- TESTHI10 – cannot be grouped with other TESTHI signals
- TESTHI12/FC44 – cannot be grouped with other TESTHI signals

Terminating multiple TESTHI pins together with a single pull-up resistor is not recommended for designs supporting boundary scan for proper Boundary Scan testing of the TESTHI signals. For optimum noise margin, all pull-up resistor values used for TESTHI[12,10:0] lands should have a resistance value within ± 20% of the impedance of the board transmission line traces. For example, if the nominal trace impedance is 50 Ω, then a value between 40 Ω and 60 Ω should be used.

2.5 Power Segment Identifier (PSID)

Power Segment Identifier (PSID) is a mechanism to prevent booting under mismatched power requirement situations. The PSID mechanism enables BIOS to detect if the processor in use requires more power than the platform voltage regulator (VR) is capable of supplying. For example, a 130 W TDP processor installed in a board with a 65 W or 95 W TDP capable VR may draw too much power and cause a potential VR issue.

2.6 Voltage and Current Specification

2.6.1 Absolute Maximum and Minimum Ratings

Table 3 specifies absolute maximum and minimum ratings only and lie outside the functional limits of the processor. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 3. Absolute Maximum and Minimum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1, 2]
V_{CC}	Core voltage with respect to V_{SS}	–0.3	1.45	V	-
V_{TT}	FSB termination voltage with respect to V_{SS}	–0.3	1.45	V	-
T_{CASE}	Processor case temperature	See Section 5	See Section 5	°C	-
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	3, 4, 5

NOTES:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, refer to the processor case temperature specifications.
4. This rating applies to the processor and does not include any tray or packaging.
5. Failure to adhere to this specification can affect the long term reliability of the processor.

2.6.2 DC Voltage and Current Specification

Table 4. Voltage and Current Specifications

Symbol	Parameter		Min	Typ	Max	Unit	Notes[2, 10]
VID Range	VID		0.8500	—	1.3625	V	1
Core V_{CC}	Processor Number (2 MB Cache): E5200 E5300	V_{CC} for 775_VR_CONFIG_06: 2.50 GHz 2.66 GHz	Refer to Table 5, Figure 1			V	3, 4, 5
V_{CC_BOOT}	Default V_{CC} voltage for initial power up		—	1.10	—	V	
V_{CCPLL}	PLL V_{CC}		- 5%	1.50	+ 5%	V	
I_{CC}	Processor Number (2 MB Cache): E5200 E5300	V_{CC} for 775_VR_CONFIG_06: 2.50 GHz 2.66 GHz	—	—	 75 75	A	6
V_{TT}	FSB termination voltage (DC + AC specifications)	on Intel 3 series Chipset family boards	1.045	1.1	1.155	V	7, 8
		on Intel 4 series Chipset family boards	1.14	1.2	1.26		
VTT_OUT_LEFT and VTT_OUT_RIGHT I_{CC}	DC Current that may be drawn from VTT_OUT_LEFT and VTT_OUT_RIGHT per land		—	—	580	mA	
I_{TT}	I_{CC} for V_{TT} supply before V_{CC} stable I_{CC} for V_{TT} supply after V_{CC} stable		—	—	4.5 4.6	A	9
I_{CC_VCCPLL}	I_{CC} for PLL land		—	—	130	mA	
I_{CC_GTLREF}	I_{CC} for GTLREF		—	—	200	µA	

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and can not be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep® technology, or Extended HALT State).
2. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
3. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.3 and Table 2 for more information.
4. The voltage specification requirements are measured across VCC_SENSE and VSS_SENSE lands at the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
5. Refer to Table 5 and Figure 1, for the minimum, typical, and maximum V_{CC} allowed for a given current. The processor should not be subjected to any V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} for a given current.
6. I_{CC_MAX} specification is based on V_{CC_MAX} loadline. Refer to Figure 1 for details.

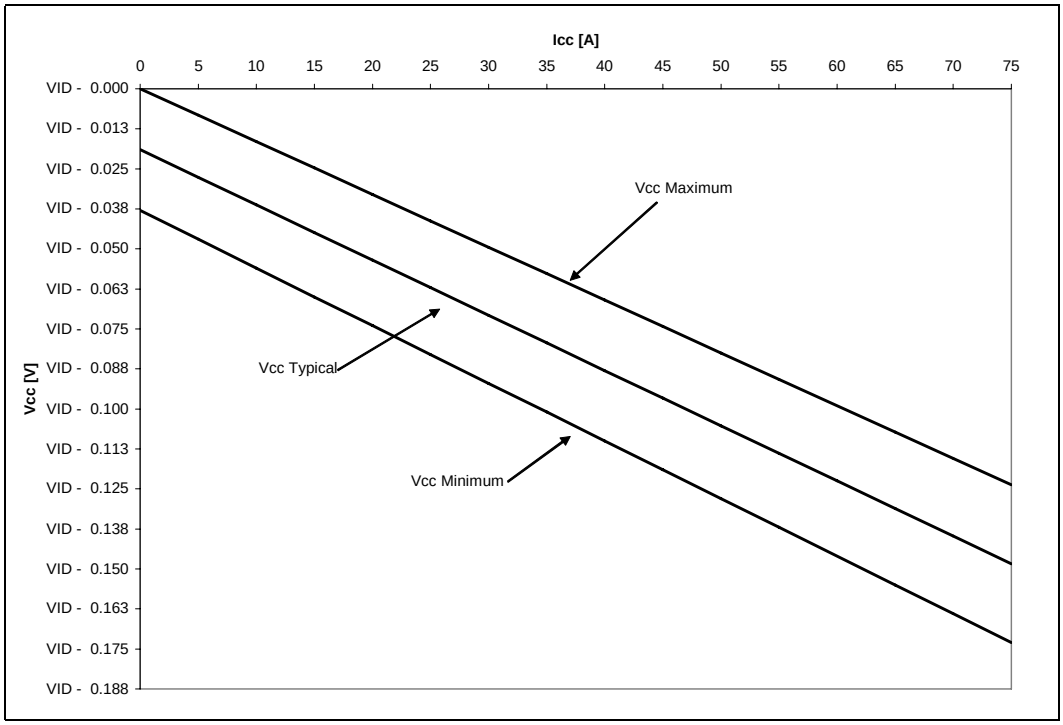
7. V_{TT} must be provided via a separate voltage source and not be connected to V_{CC}. This specification is measured at the land.
8. Baseboard bandwidth is limited to 20 MHz.
9. This is the maximum total current drawn from the V_{TT} plane by only the processor. This specification does not include the current coming from on-board termination (R_{TT}), through the signal line. Refer to the Voltage Regulator Design Guide to determine the total I_{TT} drawn by the system. This parameter is based on design characterization and is not tested.
10. Adherence to the voltage specifications for the processor are required to ensure reliable processor operation.

Table 5. Processor V_{CC} Static and Transient Tolerance

I_{CC} (A)	Voltage Deviation from VID Setting (V)[1, 2, 3, 4]		
	Maximum Voltage 1.65 mΩ	Typical Voltage 1.73 mΩ	Minimum Voltage 1.80 mΩ
0	0.000	-0.019	-0.038
5	-0.008	-0.028	-0.047
10	-0.017	-0.036	-0.056
15	-0.025	-0.045	-0.065
20	-0.033	-0.054	-0.074
25	-0.041	-0.062	-0.083
30	-0.050	-0.071	-0.092
35	-0.058	-0.079	-0.101
40	-0.066	-0.088	-0.110
45	-0.074	-0.097	-0.119
50	-0.083	-0.105	-0.128
55	-0.091	-0.114	-0.137
60	-0.099	-0.123	-0.146
65	-0.107	-0.131	-0.155
70	-0.116	-0.140	-0.164
75	-0.124	-0.148	-0.173

NOTES:
1. The loadline specification includes both static and transient limits except for overshoot allowed as shown in Section 2.6.3.
2. This table is intended to aid in reading discrete points on Figure 1.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE lands. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS lands. Refer to the Voltage Regulator Design Guide for socket loadline guidelines and VR implementation details.
4. Adherence to this loadline specification is required to ensure reliable processor operation.

Figure 1. Processor V_{CC} Static and Transient Tolerance



NOTES:
1. The loadline specification includes both static and transient limits except for overshoot allowed as shown in Section 2.6.3.
2. This loadline specification shows the deviation from the VID set point.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE lands. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS lands. Refer to the Voltage Regulator Design Guide for socket loadline guidelines and VR implementation details.

2.6.3 V_{CC} Overshoot

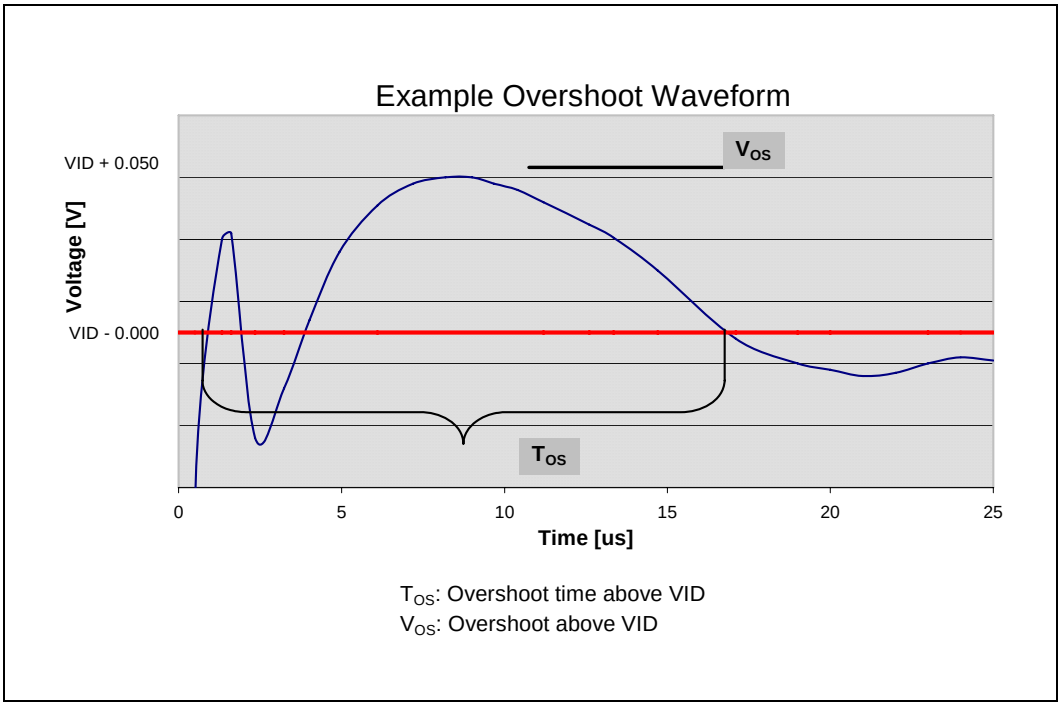
The processor can tolerate short transient overshoot events where V_{CC} exceeds the VID voltage when transitioning from a high to low current load condition. This overshoot cannot exceed VID + V_{OS_MAX} (V_{OS_MAX} is the maximum allowable overshoot voltage). The time duration of the overshoot event must not exceed T_{OS_MAX} (T_{OS_MAX} is the maximum allowable time duration above VID). These specifications apply to the processor die voltage as measured across the VCC_SENSE and VSS_SENSE lands.

Table 6. V_{CC} Overshoot Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CC} overshoot above VID	—	50	mV	2	1
T_{OS_MAX}	Time duration of V_{CC} overshoot above VID	—	25	µs	2	1

NOTES:
1. Adherence to these specifications is required to ensure reliable processor operation.

Figure 2. V_{CC} Overshoot Example Waveform



NOTES:
1. V_{OS} is measured overshoot voltage.
2. T_{OS} is measured time duration above VID.

2.6.4 Die Voltage Validation

Overshoot events on processor must meet the specifications in Table 6 when measured across the VCC_SENSE and VSS_SENSE lands. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot must be taken with a bandwidth limited oscilloscope set to a greater than or equal to 100 MHz bandwidth limit.

2.7 Signaling Specifications

Most processor Front Side Bus signals use Gunning Transceiver Logic (GTL+) signaling technology. This technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. Platforms implement a termination voltage level for GTL+ signals defined as V_{TT}. Because platforms implement separate power planes for each processor (and chipset), separate V_{CC} and V_{TT} supplies are necessary. This configuration allows for improved noise tolerance as processor frequency increases. Speed enhancements to data and address busses have caused signal integrity considerations and platform design methods to become even more critical than with previous processor families.

The GTL+ inputs require a reference voltage (GTLREF) which is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the motherboard (see Table 14 for GTLREF specifications). Termination resistors (R_{TT}) for GTL+ signals are provided on the processor silicon and are terminated to V_{TT}. Intel chipsets will also provide on-die termination, thus eliminating the need to terminate the bus on the motherboard for most GTL+ signals.

2.7.1 FSB Signal Groups

The front side bus signals have been combined into groups by buffer type. GTL+ input signals have differential input buffers, which use GTLREF[1:0] as a reference level. In this document, the term “GTL+ Input” refers to the GTL+ input group as well as the GTL+ I/O group when receiving. Similarly, “GTL+ Output” refers to the GTL+ output group as well as the GTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 7 identifies which signals are common clock, source synchronous, and asynchronous.

Table 7. FSB Signal Groups

Signal Group	Type	Signals[1]
GTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, RESET#, RS[2:0]#, TRDY#
GTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, BNR#, BPM[5:0]#, BR0#[3], DBSY#, DRDY#, HIT#, HITM#, LOCK#
GTL+ Source Synchronous I/O	Synchronous to assoc. strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#[3]</td><td>ADSTB0#</td></tr><tr><td>A[35:17]#[3]</td><td>ADSTB1#</td></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>
GTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
CMOS		A20M#, DPRSTP#. DPSLP#, IGNNE#, INIT#, LINT0/ INTR, LINT1/NMI, SMI#[3], STPCLK#, PWRGOOD, SLP#, TCK, TDI, TMS, TRST#, BSEL[2:0], VID[7:0], PSI#
Open Drain Output		FERR#/PBE#, IERR#, THERMTRIP#, TDO
Open Drain Input/ Output		PROCHOT#[4]
FSB Clock	Clock	BCLK[1:0], ITP_CLK[1:0][2]
Power/Other		VCC, VTT, VCCA, VCCIOPLL, VCCPLL, VSS, VSSA, GTLREF[1:0], COMP[8,3:0], RESERVED, TESTHI[12,10:0], VCC_SENSE, VCC_MB_REGULATION, VSS_SENSE, VSS_MB_REGULATION, DBR#[2], VTT_OUT_LEFT, VTT_OUT_RIGHT, VTT_SEL, FCx, PECI, MSID[1:0]

NOTES:
1. Refer to Section 4.2 for signal descriptions.
2. In processor systems where no debug port is implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.

3. The value of these signals during the active-to-inactive edge of RESET# defines the processor configuration options. See Section 6.1 for details.
4. PROCHOT# signal type is open drain output and CMOS input.

Table 8. Signal Characteristics

Signals with R_{TT}	Signals with No R_{TT}
A[35:3]#, ADS#, ADSTB[1:0]#, BNR#, BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, HIT#, HITM#, LOCK#, PROCHOT#, REQ[4:0]#, RS[2:0]#, TRDY#	A20M#, BCLK[1:0], BPM[5:0]#, BSEL[2:0], COMP[8,3:0], FERR#/PBE#, IERR#, IGNNE#, INIT#, ITP_CLK[1:0], LINT0/INTR, LINT1/NMI, MSID[1:0], PWRGOOD, RESET#, SMI#, STPCLK#, TDO, TESTHI[12,10:0], THERMTRIP#, VID[7:0], GTLREF[1:0], TCK, TDI, TMS, TRST#, VTT_SEL
Open Drain Signals[1]	
THERMTRIP#, FERR#/PBE#, IERR#, BPM[5:0]#, BR0#, TDO, FCx	

NOTES:
1. Signals that do not have R_{TT}, nor are actively driven to their high-voltage level.

Table 9. Signal Reference Voltages

GTLREF	V_{TT} / 2
BPM[5:0]#, RESET#, BNR#, HIT#, HITM#, BR0#, A[35:0]#, ADS#, ADSTB[1:0]#, BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, LOCK#, REQ[4:0]#, RS[2:0]#, TRDY#	A20M#, LINT0/INTR, LINT1/NMI, IGNNE#, INIT#, PROCHOT#, PWRGOOD[1], SMI#, STPCLK#, TCK[1], TDI[1], TMS[1], TRST#[1]

NOTE:
1. See Table 11 for more information.

2.7.2 CMOS and Open Drain Signals

Legacy input signals such as A20M#, IGNNE#, INIT#, SMI#, and STPCLK# use CMOS input buffers. All of the CMOS and Open Drain signals are required to be asserted/de-asserted for at least eight BCLKs in order for the processor to recognize the proper signal state. See Section 2.7.3 for the DC specifications. See Section 6.2 for additional timing requirements for entering and leaving the low power states.

2.7.3 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless otherwise stated. All specifications apply to all frequencies and cache sizes unless otherwise stated.

Table 10. GTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	-0.10	GTLREF – 0.10	V	2, 5
V_{IH}	Input High Voltage	GTLREF + 0.10	V_{TT} + 0.10	V	3, 4, 5
V_{OH}	Output High Voltage	V_{TT} – 0.10	V_{TT}	V	4, 5
I_{OL}	Output Low Current	N/A	V_{TT_MAX} / [(R_{TT_MIN}) + (2 * R_{ON_MIN})]	A	-
I_{LI}	Input Leakage Current	N/A	± 100	µA	6
I_{LO}	Output Leakage Current	N/A	± 100	µA	7
R_{ON}	Buffer On Resistance	7.49	9.16	Ω	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{TT}.
5. The V_{TT} referred to in these specifications is the instantaneous V_{TT}.
6. Leakage to V_{SS} with land held at V_{TT}.
7. Leakage to V_{TT} with land held at 300 mV.

Table 11. Open Drain and TAP Output Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{OL}	Output Low Voltage	0	0.20	V	-
I_{OL}	Output Low Current	16	50	mA	2
I_{LO}	Output Leakage Current	N/A	± 200	µA	3

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at V_{TT} * 0.2 V.
3. For Vin between 0 and V_{OH}.

Table 12. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	-0.10	V_{TT} * 0.30	V	3, 6
V_{IH}	Input High Voltage	V_{TT} * 0.70	V_{TT} + 0.10	V	4, 5, 6
V_{OL}	Output Low Voltage	-0.10	V_{TT} * 0.10	V	6
V_{OH}	Output High Voltage	0.90 * V_{TT}	V_{TT} + 0.10	V	2, 5, 6
I_{OL}	Output Low Current	V_{TT} * 0.10 / 67	V_{TT} * 0.10 / 27	A	6, 7
I_{OH}	Output Low Current	V_{TT} * 0.10 / 67	V_{TT} * 0.10 / 27	A	6, 7
I_{LI}	Input Leakage Current	N/A	± 100	µA	8
I_{LO}	Output Leakage Current	N/A	± 100	µA	9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open drain.
3. V_{IL} is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
4. V_{IH} is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{TT}.
6. The V_{TT} referred to in these specifications refers to instantaneous V_{TT}.
7. I_{OL} is measured at 0.10 * V_{TT}. I_{OH} is measured at 0.90 * V_{TT}.
8. Leakage to V_{SS} with land held at V_{TT}.
9. Leakage to V_{TT} with land held at 300 mV.

2.7.3.1 Platform Environment Control Interface (PECI) DC Specifications

PECI is an Intel proprietary one-wire interface that provides a communication channel between Intel processors, chipsets, and external thermal monitoring devices. The processor contains Digital Thermal Sensors (DTS) distributed throughout die. These sensors are implemented as analog-to-digital converters calibrated at the factory for reasonable accuracy to provide a digital representation of relative processor temperature. PECI provides an interface to relay the highest DTS temperature within a die to external management devices for thermal/fan speed control. More detailed information may be found in the *Platform Environment Control Interface (PECI) Specification.*

Table 13. PECI DC Electrical Limits

Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
V_{in}	Input Voltage Range	-0.15	V_{TT}	V	
$V_{hysteresis}$	Hysteresis	0.1 * V_{TT}	—	V	[2]
V_n	Negative-edge threshold voltage	0.275 * V_{TT}	0.500 * V_{TT}	V	
V_p	Positive-edge threshold voltage	0.550 * V_{TT}	0.725 * V_{TT}	V	
I_{source}	High level output source (V_{OH} = 0.75 * V_{TT})	-6.0	N/A	mA	
I_{sink}	Low level output sink (V_{OL} = 0.25 * V_{TT})	0.5	1.0	mA	
I_{leak+}	High impedance state leakage to V_{TT}	N/A	50	µA	[3]
I_{leak-}	High impedance leakage to GND	N/A	10	µA	3
C_{bus}	Bus capacitance per node	N/A	10	pF	4
V_{noise}	Signal noise immunity above 300 MHz	0.1 * V_{TT}	—	V_{p-p}	

NOTES:
1. V_{TT} supplies the PECI interface. PECI behavior does not affect V_{TT} min/max specifications. Refer to Table 4 for V_{TT} specifications.
2. The leakage specification applies to powered devices on the PECI bus.
3. The input buffers use a Schmitt-triggered input design for improved noise immunity.
4. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.

2.7.3.2 GTL+ Front Side Bus Specifications

In most cases, termination resistors are not required as these are integrated into the processor silicon. See Table 8 for details on which GTL+ signals do not include on-die termination.

Valid high and low levels are determined by the input buffers by comparing with a reference voltage called GTLREF. Table 14 lists the GTLREF specifications. The GTL+ reference voltage (GTLREF) should be generated on the system board using high precision voltage divider circuits.

Table 14. GTL+ Bus Voltage Definitions

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
GTLREF_PU	GTLREF pull up on Intel® 3 Series Chipset family boards	57.6 * 0.99	57.6	57.6 * 1.01	Ω	2
GTLREF_PD	GTLREF pull down on Intel® 3 Series Chipset family boards	100 * 0.99	100	100 * 1.01	Ω	2
R_{TT}	Termination Resistance	45	50	55	Ω	3
COMP[3:0]	COMP Resistance	49.40	49.90	50.40	Ω	4
COMP8	COMP Resistance	24.65	24.90	25.15	Ω	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. GTLREF is to be generated from V_{TT} by a voltage divider of 1% resistors. If an Adjustable GTLREF circuit is used on the board (for Quad-Core processors compatibility) the two GTLREF lands connected to the Adjustable GTLREF circuit require the following: GTLREF_PU = 50 Ω, GTLREF_PD = 100 Ω.
3. R_{TT} is the on-die termination resistance measured at V_{TT}/3 of the GTL+ output driver.
4. COMP resistance must be provided on the system board with 1% resistors. COMP[3:0] and COMP8 resistors are to V_{SS}.

2.8 Clock Specifications

2.8.1 Front Side Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous generation processors, the processor's core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier will be set at its default ratio during manufacturing. The processor supports Half Ratios between 7.5 and 13.5, refer to Table 15 for the processor supported ratios.

The processor uses a differential clocking implementation. For more information on the processor clocking, contact your Intel field representative.

Table 15. Core Frequency to FSB Multiplier Configuration

Multiplication of System Core Frequency to FSB Frequency	Core Frequency (200 MHz BCLK/800 MHz FSB)	Notes[1, 2]
1/6	1.20 GHz	-
1/7	1.40 GHz	-
1/7.5	1.5 GHz	-
1/8	1.60 GHz	-
1/8.5	1.70 GHz	-
1/9	1.80 GHz	-
1/9.5	1.90 GHz	-
1/10	2 GHz	-
1/10.5	2.1 GHz	-
1/11	2.2 GHz	-
1/11.5	2.3 GHz	-
1/12	2.4 GHz	-
1/12.5	2.5 GHz	-
1/13	2.6 GHz	-
1/13.5	2.7 GHz	-
1/14	2.8 GHz	-
1/15	3 GHz	-

NOTES:
1. Individual processors operate only at or below the rated frequency.
2. Listed frequencies are not necessarily committed production frequencies.

2.8.2 FSB Frequency Select Signals (BSEL[2:0])

The BSEL[2:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). Table 16 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset, and clock synthesizer. All agents must operate at the same frequency.

The processor operates at a 800 MHz FSB frequency (selected by a 200 MHz BCLK[1:0] frequency). Individual processors will only operate at their specified FSB frequency.

For more information about these signals, refer to Section 4.2.

Table 16. BSEL[2:0] Frequency Table for BCLK[1:0]

BSEL2	BSEL1	BSEL0	FSB Frequency
L	L	L	Rerserved
L	L	H	Rerserved
L	H	H	Rerserved
L	H	L	200 MHz
H	H	L	Rerserved
H	H	H	Rerserved
H	L	H	Rerserved
H	L	L	Rerserved

2.8.3 Phase Lock Loop (PLL) and Filter

An on-die PLL filter solution will be implemented on the processor. The VCCPLL input is used for the PLL. Refer to Table 4 for DC specifications.

2.8.4 BCLK[1:0] Specifications

Table 17. Front Side Bus Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes[1]
V_L	Input Low Voltage	-0.30	N/A	N/A	V	3	
V_H	Input High Voltage	N/A	N/A	1.15	V	3	
$V_{CROSS(abs)}$	Absolute Crossing Point	0.300	N/A	0.550	V	3	2
ΔV_{CROSS}	Range of Crossing Points	N/A	N/A	0.140	V	3	-
V_{OS}	Overshoot	N/A	N/A	1.4	V	3	3
V_{US}	Undershoot	-0.300	N/A	N/A	V	3	3
V_{SWING}	Differential Output Swing	0.300	N/A	N/A	V	4	4

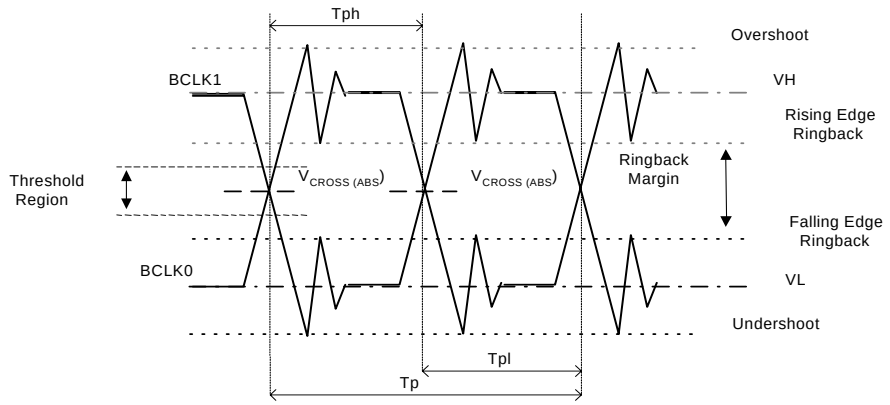
NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing voltage is defined as the instantaneous voltage value when the rising edge of BCLK0 equals the falling edge of BCLK1.
3. “Steady state” voltage, not including overshoot or undershoot.
4. Overshoot is defined as the absolute value of the maximum voltage. Undershoot is defined as the absolute value of the minimum voltage.
5. Measurement taken from differential waveform.

Table 18. FSB Differential Clock Specifications (800 MHz FSB)

T# Parameter	Min	Nom	Max	Unit	Figure	Notes[1]
BCLK[1:0] Frequency	198.980	—	200.020	MHz	-	2
T1: BCLK[1:0] Period	4.99950	—	5.00050	ns	3	3
T2: BCLK[1:0] Period Stability	—	—	150	ps	3	4
T5: BCLK[1:0] Rise and Fall Slew Rate	2.5	—	8	V/nS	3	5
T6: Slew Rate Matching	N/A	N/A	20	%		6

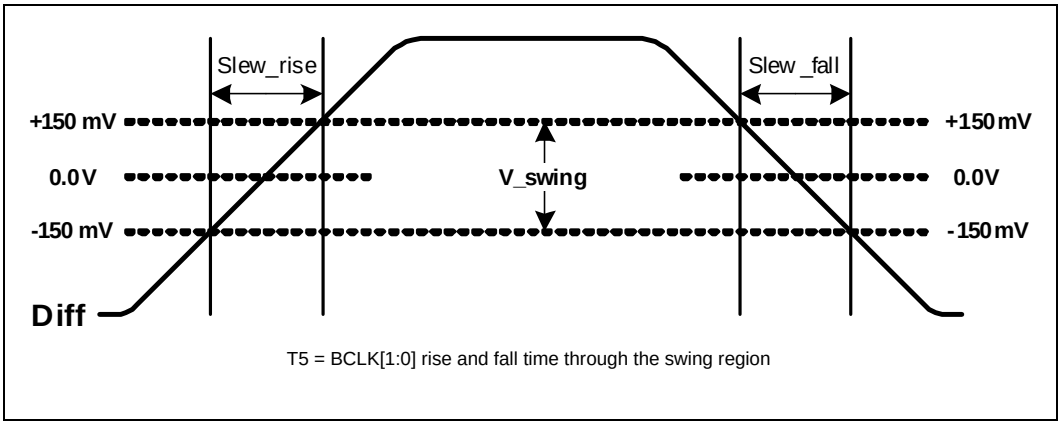
NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor core frequencies based on a 200 MHz BCLK[1:0].
2. Duty Cycle (High time/Period) must be between 40 and 60%.
3. The period specified here is the average period. A given period may vary from this specification as governed by the period stability specification (T2). Min period specification is based on -300 PPM deviation from a 5 ns period. Max period specification is based on the summation of +300 PPM deviation from a 5 ns period and a +0.5% maximum variance due to spread spectrum clocking.
4. In this context, period stability is defined as the worst case timing difference between successive crossover voltages. In other words, the largest absolute difference between adjacent clock periods must be less than the period stability.
5. Measurement taken from differential waveform.
6. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75 mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. Slew rate matching is a single ended measurement.

Figure 3. Differential Clock Waveform



Tp = T1: BCLK[1:0] period
T2: BCLK[1:0] period stability (not shown)
Tph = T3: BCLK[1:0] pulse high time
Tpl = T4: BCLK[1:0] pulse low time
T5: BCLK[1:0] rise time through the threshold region
T6: BCLK[1:0] fall time through the threshold region

Figure 4. Measurement Points for Differential Clock Waveforms



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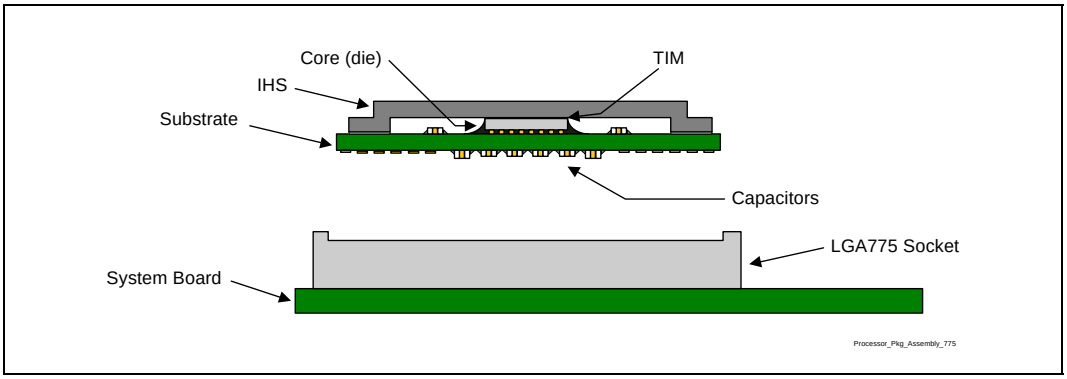
3 Package Mechanical Specifications

The processor is packaged in a Flip-Chip Land Grid Array (FC-LGA8) package that interfaces with the motherboard via an LGA775 socket. The package consists of a processor core mounted on a substrate land-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions, such as a heatsink. Figure 5 shows a sketch of the processor package components and how they are assembled together. Refer to the *LGA775 Socket Mechanical Design Guide* for complete details on the LGA775 socket.

The package components shown in Figure 5 include the following:

- Integrated Heat Spreader (IHS)
- Thermal Interface Material (TIM)
- Processor core (die)
- Package substrate
- Capacitors

Figure 5. Processor Package Assembly Sketch



NOTE:
1. Socket and motherboard are included for reference and are not part of processor package.

3.1 Package Mechanical Drawing

The package mechanical drawings are shown in Figure 6 and Figure 7. The drawings include dimensions necessary to design a thermal solution for the processor. These dimensions include:

- Package reference with tolerances (total height, length, width, etc.)
- IHS parallelism and tilt
- Land dimensions
- Top-side and back-side component keep-out dimensions
- Reference datums
- All drawing dimensions are in mm [in].
- Guidelines on potential IHS flatness variation with socket load plate actuation and installation of the cooling solution is available in the processor Thermal and Mechanical Design Guidelines.

Figure 6. Processor Package Drawing Sheet 1 of 3

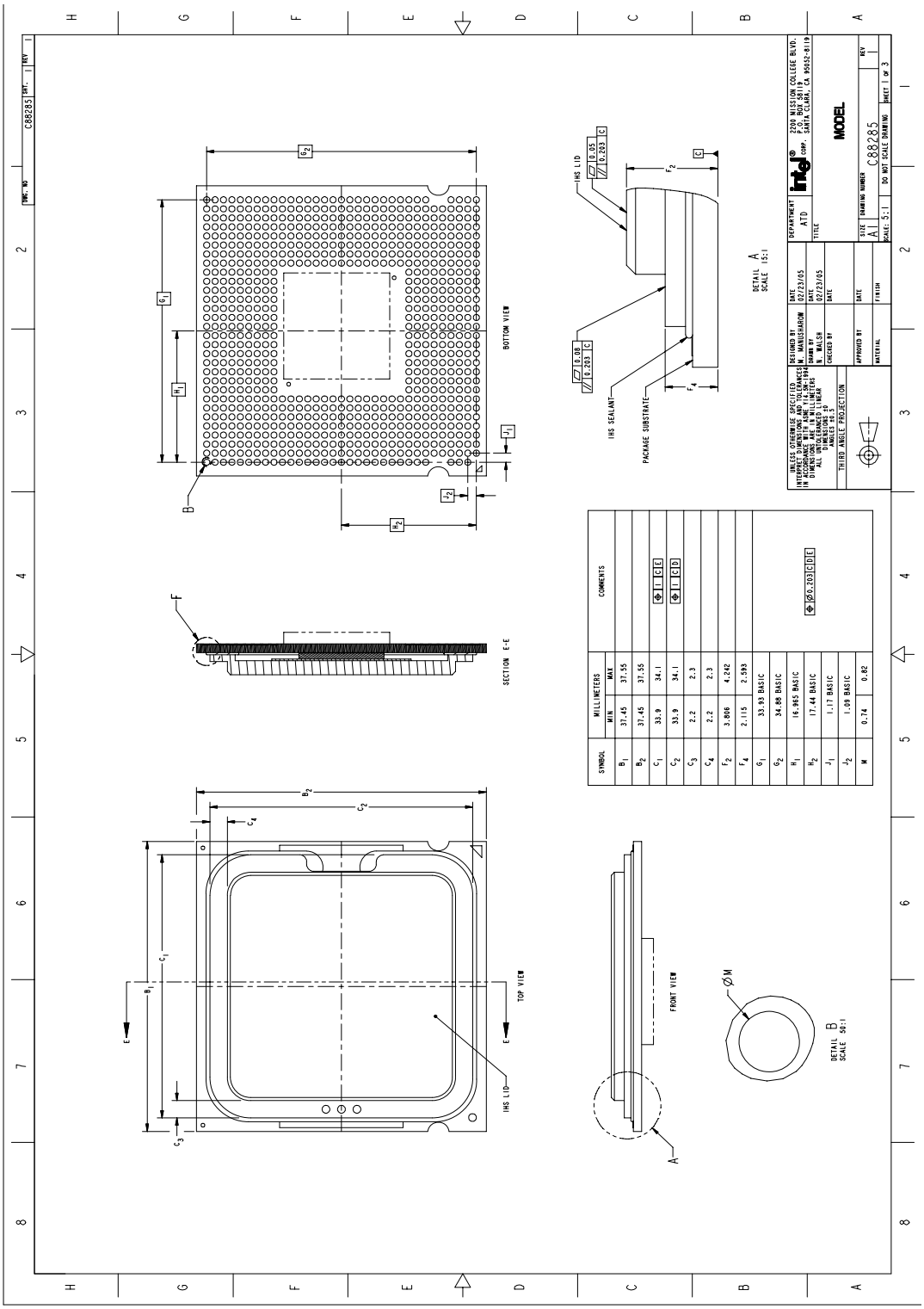


Figure 7. Processor Package Drawing Sheet 2 of 3

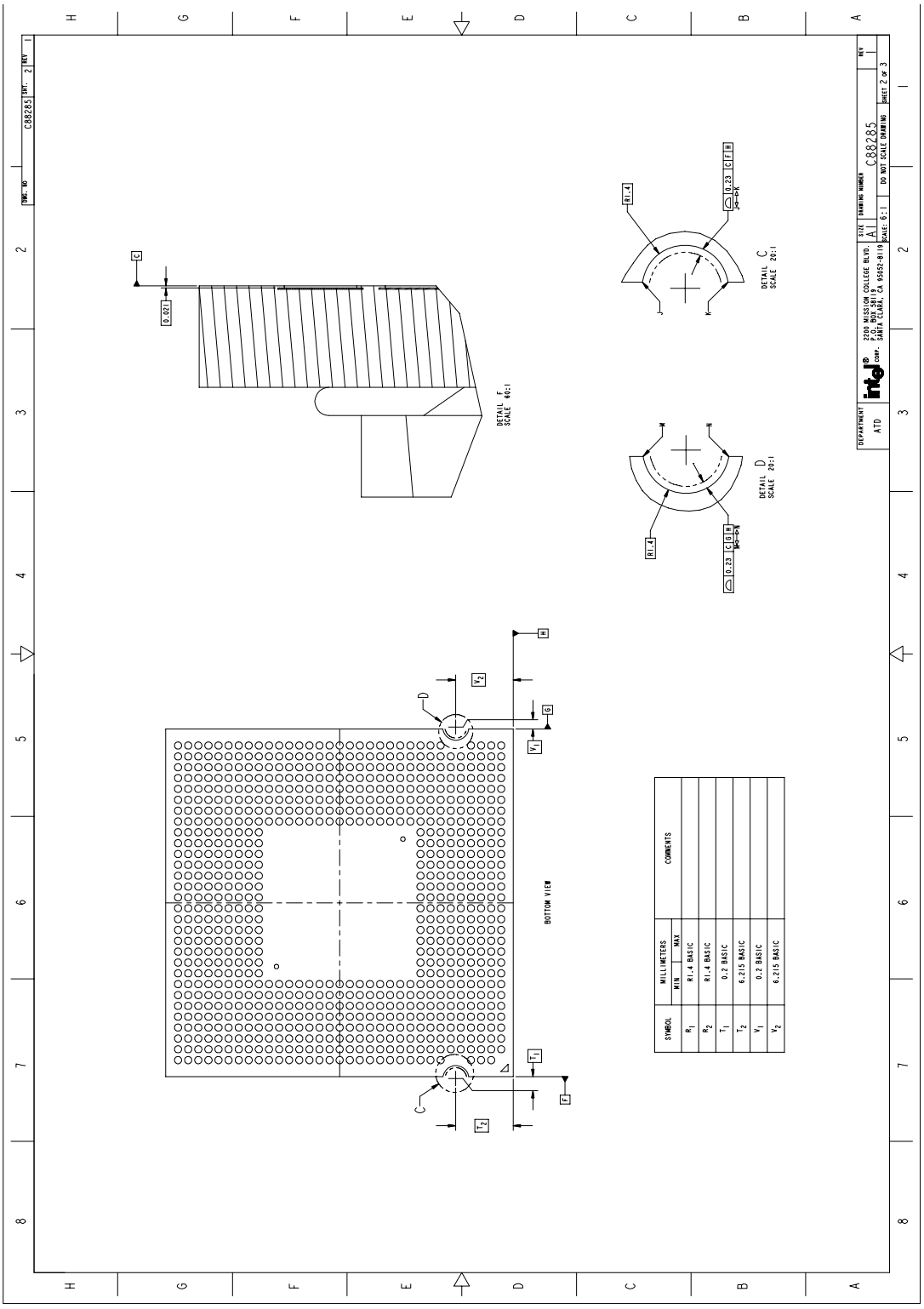
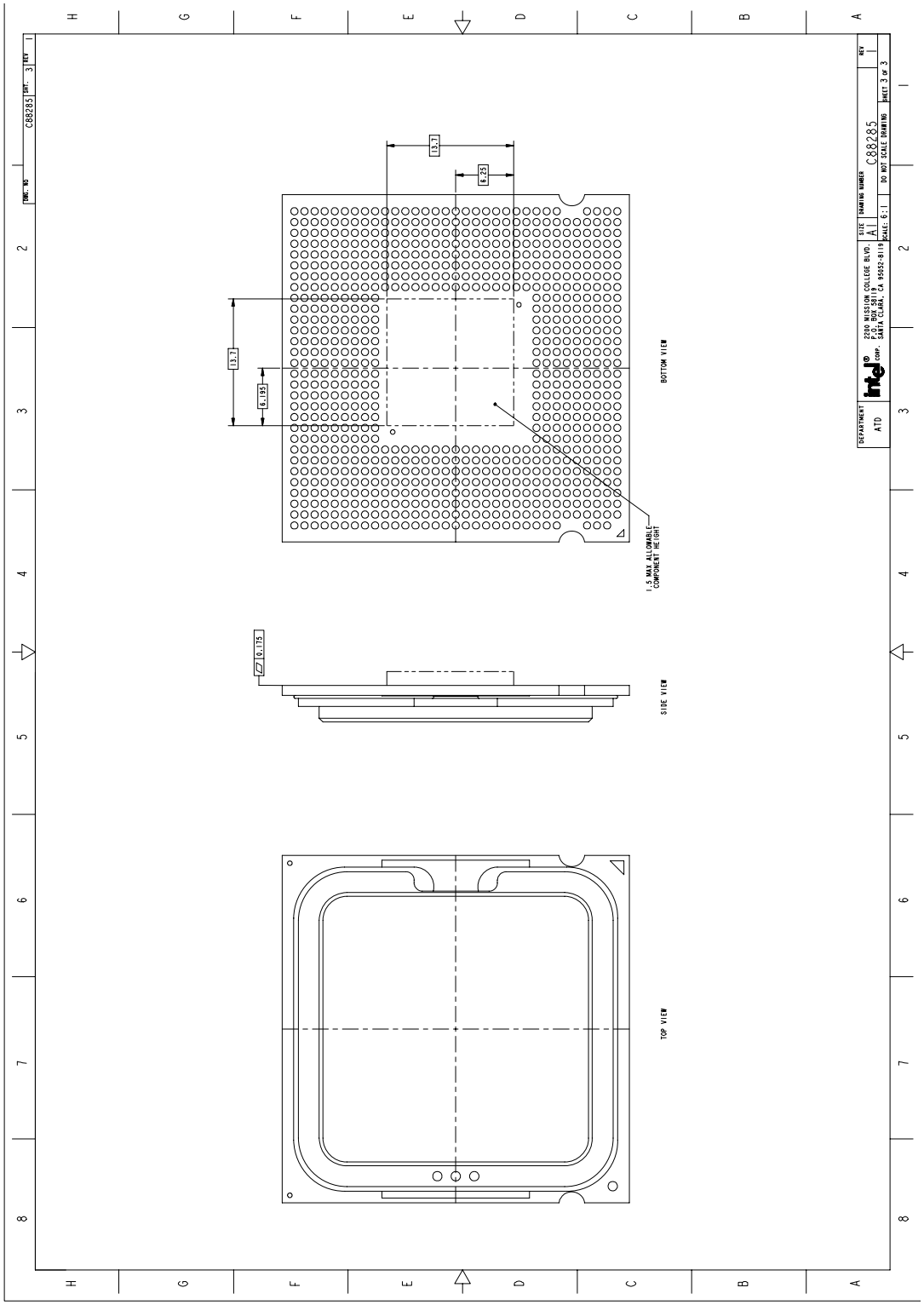


Figure 8. Processor Package Drawing Sheet 3 of 3



3.2 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted to either the topside or land-side of the package substrate. See Figure 6 and Figure 7 for keep-out zones. The location and quantity of package capacitors may change due to manufacturing efficiencies but will remain within the component keep-in.

3.3 Package Loading Specifications

Table 19 provides dynamic and static load specifications for the processor package. These mechanical maximum load limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Also, any mechanical system or component testing should not exceed the maximum limits. The processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal and mechanical solution. The minimum loading specification must be maintained by any thermal and mechanical solutions.

Table 19. Processor Loading Specifications

Parameter	Minimum	Maximum	Notes
Static	80 N [17 lbf]	311 N [70 lbf]	1, 2, 3
Dynamic	-	756 N [170 lbf]	1, 3, 4

NOTES:
1. These specifications apply to uniform compressive loading in a direction normal to the processor IHS.
2. This is the maximum force that can be applied by a heatsink retention clip. The clip must also provide the minimum specified load on the processor package.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only and do not include the limits of the processor socket.
4. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.

3.4 Package Handling Guidelines

Table 20 includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 20. Package Handling Guidelines

Parameter	Maximum Recommended	Notes
Shear	311 N [70 lbf]	1, 4
Tensile	111 N [25 lbf]	2, 4
Torque	3.95 N-m [35 lbf-in]	3, 4

NOTES:
1. A shear load is defined as a load applied to the IHS in a direction parallel to the IHS top surface.
2. A tensile load is defined as a pulling load applied to the IHS in a direction normal to the IHS surface.
3. A torque load is defined as a twisting load applied to the IHS in an axis of rotation normal to the IHS top surface.
4. These guidelines are based on limited testing for design characterization.

3.5 Package Insertion Specifications

The processor can be inserted into and removed from a LGA775 socket 15 times. The socket should meet the LGA775 requirements detailed in the *LGA775 Socket Mechanical Design Guide*.

3.6 Processor Mass Specification

The typical mass of the processor is 21.5 g [0.76 oz]. This mass [weight] includes all the components that are included in the package.

3.7 Processor Materials

Table 21 lists some of the package components and associated materials.

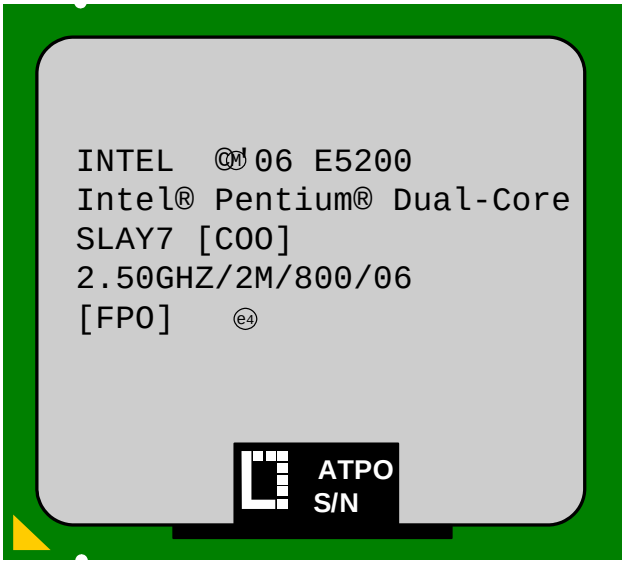
Table 21. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel Plated Copper
Substrate	Fiber Reinforced Resin
Substrate Lands	Gold Plated Copper

3.8 Processor Markings

Figure 9 shows the topside markings on the processor. This diagram is to aid in the identification of the processor.

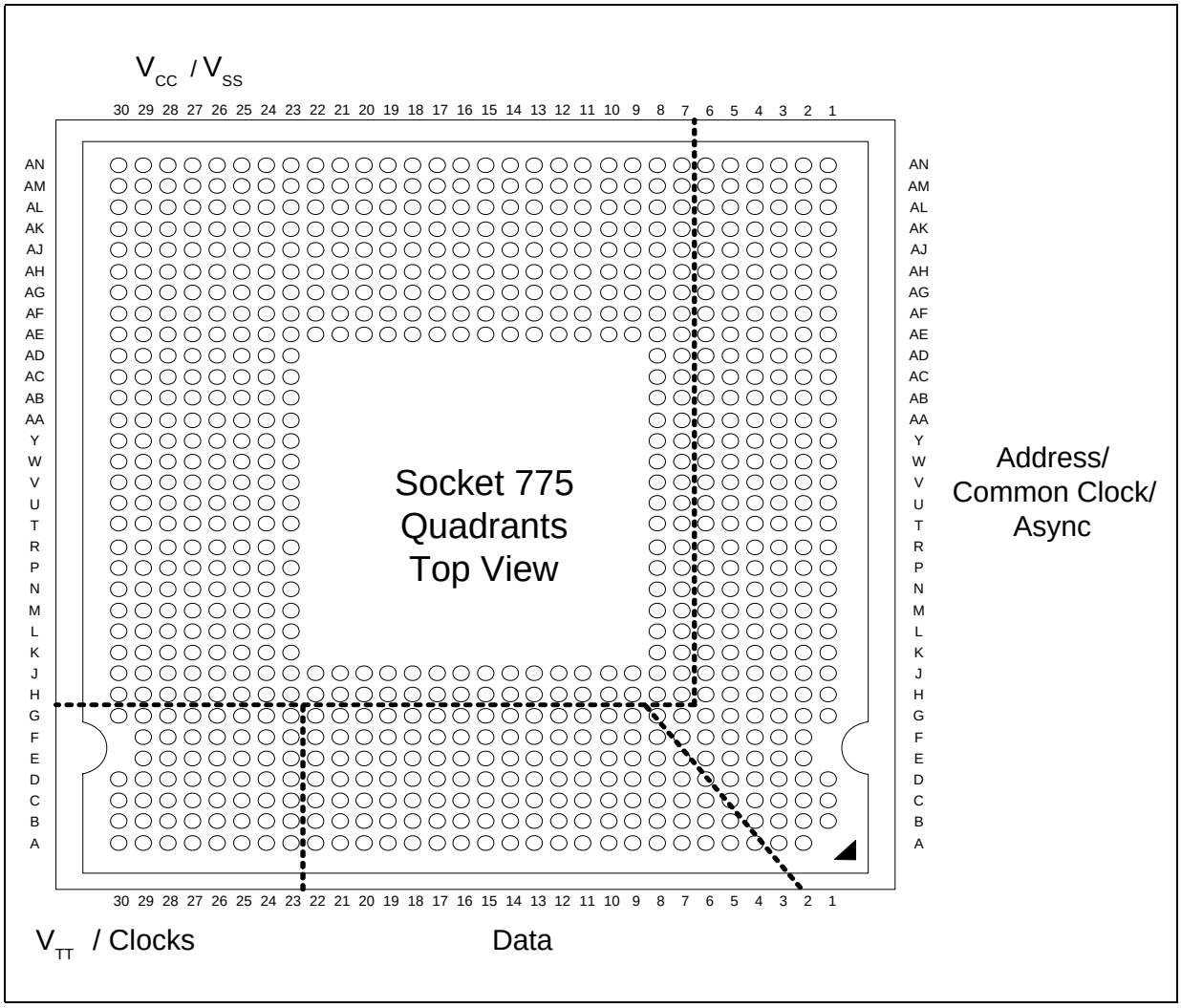
Figure 9. Processor Top-Side Markings Example



3.9 Processor Land Coordinates

Figure 10 shows the top view of the processor land coordinates. The coordinates are referred to throughout the document to identify processor lands.

Figure 10. Processor Land Coordinates and Quadrants, Top View


VCC / VSS
30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
AN AM AL AK AJ AH AG AF AE AD AC AB AA Y W V U T R P N M L K J H G F E D C B A
Socket 775
Quadrants
Top View
Address/
Common Clock/
Async
VTT / Clocks
Data

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4 Land Listing and Signal Descriptions

This chapter provides the processor land assignment and signal descriptions.

4.1 Processor Land Assignments

This section contains the land listings for the processor. The land-out footprint is shown in Figure 11 and Figure 12. These figures represent the land-out arranged by land number and they show the physical location of each signal on the package land array (top view). Table 22 lists the processor lands ordered alphabetically by land (signal) name. Table 23 lists the processor lands ordered numerically by land number.

Figure 11. land-out Diagram (Top View – Left Side)

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15
AN	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AM	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AL	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AK	VSS	VSS	VSS	VSS	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AJ	VSS	VSS	VSS	VSS	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AH	VCC	VCC	VCC	VCC	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AG	VCC	VCC	VCC	VCC	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AF	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AB	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
AA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
Y	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
W	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
U	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
T	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
R	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
P	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
N	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
M	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
L	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
K	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
J	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	FC34	FC31	VCC
H	BSEL1	FC15	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	FC33	FC32
G	BSEL2	BSEL0	BCLK1	TESTHI4	TESTHI5	TESTHI3	TESTHI6	RESET#	D47#	D44#	DSTBN2#	DSTBP2#	D35#	D36#	D32#	D31#
F		RSVD	BCLK0	VTT_SEL	TESTHI0	TESTHI2	TESTHI7	RSVD	VSS	D43#	D41#	VSS	D38#	D37#	VSS	D30#
E		FC26	VSS	VSS	VSS	VSS	FC10	RSVD	D45#	D42#	VSS	D40#	D39#	VSS	D34#	D33#
D	VTT	VTT	VTT	VTT	VTT	VTT	VSS	VCCPLL	D46#	VSS	D48#	DBI2#	VSS	D49#	RSVD	VSS
C	VTT	VTT	VTT	VTT	VTT	VTT	VSS	VCCIO PLL	VSS	D58#	DBI3#	VSS	D54#	DSTBP3#	VSS	D51#
B	VTT	VTT	VTT	VTT	VTT	VTT	VSS	VSSA	D63#	D59#	VSS	D60#	D57#	VSS	D55#	D53#
A	VTT	VTT	VTT	VTT	VTT	VTT	FC23	VCCA	D62#	VSS	RSVD	D61#	VSS	D56#	DSTBN3#	VSS
	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15

Figure 12. land-out Diagram (Top View – Right Side)

14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VID_SELECT	VSS_MB_REGULATION	VCC_MB_REGULATION	VSS_SENSE	VCC_SENSE	VSS	VSS	AN
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VID7	FC40	VID6	VSS	VID2	VID0	VSS	AM
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VID3	VID1	VID5	VRDSEL	PROCHOT#	FC25	AL
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	FC8	VSS	VID4	ITP_CLK0	VSS	FC24	AK
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	A35#	A34#	VSS	ITP_CLK1	BPM0#	BPM1#	AJ
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	A33#	A32#	VSS	RSVD	VSS	AH
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	A29#	A31#	A30#	BPM5#	BPM3#	TRST#	AG
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	A27#	A28#	VSS	BPM4#	TDO	AF
VCC	VSS	VCC	VCC	VSS	VCC	SKTOCC#	VSS	RSVD	VSS	RSVD	FC18	VSS	TCK	AE
						VCC	VSS	A22#	ADSTB1#	VSS	FC36	BPM2#	TDI	AD
						VCC	VSS	VSS	A25#	RSVD	VSS	DBR#	TMS	AC
						VCC	VSS	A17#	A24#	A26#	FC37	IERR#	VSS	AB
						VCC	VSS	VSS	A23#	A21#	VSS	FC39	VTT_OUT_RIGHT	AA
						VCC	VSS	A19#	VSS	A20#	PSII#	VSS	FC0/ BOOTSELECT	Y
						VCC	VSS	A18#	A16#	VSS	TESTHI1	TESTHI12/ FC44	MSID0	W
						VCC	VSS	VSS	A14#	A15#	VSS	RSVD	MSID1	V
						VCC	VSS	A10#	A12#	A13#	FC30	FC29	FC28	U
						VCC	VSS	VSS	A9#	A11#	VSS	DPRSTP#	COMP1	T
						VCC	VSS	ADSTB0#	VSS	A8#	FERR#/ PBE#	VSS	COMP3	R
						VCC	VSS	A4#	RSVD	VSS	INIT#	SMI#	DPSLP#	P
						VCC	VSS	VSS	RSVD	RSVD	VSS	IGNNE#	PWRGOOD	N
						VCC	VSS	REQ2#	A5#	A7#	STPCLK#	THERMTRIP#	VSS	M
						VCC	VSS	VSS	A3#	A6#	VSS	SLP#	LINT1	L
						VCC	VSS	REQ3#	VSS	REQ0#	A20M#	VSS	LINT0	K
VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS	REQ4#	REQ1#	VSS	FC22	FC3	VTT_OUT_LEFT	J
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	TESTHI10	FC35	VSS	GTLREF1	GTLREF0	H
D29#	D27#	DSTBN1#	DBI1#	FC38	D16#	BPRI#	DEFER#	RSVD	PECI	TESTHI9/ FC43	TESTHI8/ FC42	COMP2	FC27	G
D28#	VSS	D24#	D23#	VSS	D18#	D17#	VSS	FC21	RS1#	VSS	BR0#	FC5		F
VSS	D26#	DSTBP1#	VSS	D21#	D19#	VSS	RSVD	RSVD	FC20	HITM#	TRDY#	VSS		E
RSVD	D25#	VSS	D15#	D22#	VSS	D12#	D20#	VSS	VSS	HIT#	VSS	ADS#	RSVD	D
D52#	VSS	D14#	D11#	VSS	FC41	DSTBN0#	VSS	D3#	D1#	VSS	LOCK#	BNR#	DRDY#	C
VSS	COMP8	D13#	VSS	D10#	DSTBP0#	VSS	D6#	D5#	VSS	D0#	RS0#	DBSY#	VSS	B
D50#	COMP0	VSS	D9#	D8#	VSS	DBI0#	D7#	VSS	D4#	D2#	RS2#	VSS		A
14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
A3#	L5	Source Synch	Input/Output
A4#	P6	Source Synch	Input/Output
A5#	M5	Source Synch	Input/Output
A6#	L4	Source Synch	Input/Output
A7#	M4	Source Synch	Input/Output
A8#	R4	Source Synch	Input/Output
A9#	T5	Source Synch	Input/Output
A10#	U6	Source Synch	Input/Output
A11#	T4	Source Synch	Input/Output
A12#	U5	Source Synch	Input/Output
A13#	U4	Source Synch	Input/Output
A14#	V5	Source Synch	Input/Output
A15#	V4	Source Synch	Input/Output
A16#	W5	Source Synch	Input/Output
A17#	AB6	Source Synch	Input/Output
A18#	W6	Source Synch	Input/Output
A19#	Y6	Source Synch	Input/Output
A20#	Y4	Source Synch	Input/Output
A21#	AA4	Source Synch	Input/Output
A22#	AD6	Source Synch	Input/Output
A23#	AA5	Source Synch	Input/Output
A24#	AB5	Source Synch	Input/Output
A25#	AC5	Source Synch	Input/Output
A26#	AB4	Source Synch	Input/Output
A27#	AF5	Source Synch	Input/Output
A28#	AF4	Source Synch	Input/Output
A29#	AG6	Source Synch	Input/Output
A30#	AG4	Source Synch	Input/Output
A31#	AG5	Source Synch	Input/Output
A32#	AH4	Source Synch	Input/Output
A33#	AH5	Source Synch	Input/Output
A34#	AJ5	Source Synch	Input/Output
A35#	AJ6	Source Synch	Input/Output
A20M#	K3	Asynch CMOS	Input
ADS#	D2	Common Clock	Input/Output
ADSTB0#	R6	Source Synch	Input/Output
ADSTB1#	AD5	Source Synch	Input/Output
BCLK0	F28	Clock	Input
BCLK1	G28	Clock	Input

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
BNR#	C2	Common Clock	Input/Output
BPM0#	AJ2	Common Clock	Input/Output
BPM1#	AJ1	Common Clock	Input/Output
BPM2#	AD2	Common Clock	Input/Output
BPM3#	AG2	Common Clock	Input/Output
BPM4#	AF2	Common Clock	Input/Output
BPM5#	AG3	Common Clock	Input/Output
BPRI#	G8	Common Clock	Input
BR0#	F3	Common Clock	Input/Output
BSEL0	G29	Asynch CMOS	Output
BSEL1	H30	Asynch CMOS	Output
BSEL2	G30	Asynch CMOS	Output
COMP0	A13	Power/Other	Input
COMP1	T1	Power/Other	Input
COMP2	G2	Power/Other	Input
COMP3	R1	Power/Other	Input
COMP8	B13	Power/Other	Input
D0#	B4	Source Synch	Input/Output
D1#	C5	Source Synch	Input/Output
D2#	A4	Source Synch	Input/Output
D3#	C6	Source Synch	Input/Output
D4#	A5	Source Synch	Input/Output
D5#	B6	Source Synch	Input/Output
D6#	B7	Source Synch	Input/Output
D7#	A7	Source Synch	Input/Output
D8#	A10	Source Synch	Input/Output
D9#	A11	Source Synch	Input/Output
D10#	B10	Source Synch	Input/Output
D11#	C11	Source Synch	Input/Output
D12#	D8	Source Synch	Input/Output
D13#	B12	Source Synch	Input/Output
D14#	C12	Source Synch	Input/Output
D15#	D11	Source Synch	Input/Output
D16#	G9	Source Synch	Input/Output
D17#	F8	Source Synch	Input/Output
D18#	F9	Source Synch	Input/Output
D19#	E9	Source Synch	Input/Output
D20#	D7	Source Synch	Input/Output
D21#	E10	Source Synch	Input/Output

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
D22#	D10	Source Synch	Input/Output
D23#	F11	Source Synch	Input/Output
D24#	F12	Source Synch	Input/Output
D25#	D13	Source Synch	Input/Output
D26#	E13	Source Synch	Input/Output
D27#	G13	Source Synch	Input/Output
D28#	F14	Source Synch	Input/Output
D29#	G14	Source Synch	Input/Output
D30#	F15	Source Synch	Input/Output
D31#	G15	Source Synch	Input/Output
D32#	G16	Source Synch	Input/Output
D33#	E15	Source Synch	Input/Output
D34#	E16	Source Synch	Input/Output
D35#	G18	Source Synch	Input/Output
D36#	G17	Source Synch	Input/Output
D37#	F17	Source Synch	Input/Output
D38#	F18	Source Synch	Input/Output
D39#	E18	Source Synch	Input/Output
D40#	E19	Source Synch	Input/Output
D41#	F20	Source Synch	Input/Output
D42#	E21	Source Synch	Input/Output
D43#	F21	Source Synch	Input/Output
D44#	G21	Source Synch	Input/Output
D45#	E22	Source Synch	Input/Output
D46#	D22	Source Synch	Input/Output
D47#	G22	Source Synch	Input/Output
D48#	D20	Source Synch	Input/Output
D49#	D17	Source Synch	Input/Output
D50#	A14	Source Synch	Input/Output
D51#	C15	Source Synch	Input/Output
D52#	C14	Source Synch	Input/Output
D53#	B15	Source Synch	Input/Output
D54#	C18	Source Synch	Input/Output
D55#	B16	Source Synch	Input/Output
D56#	A17	Source Synch	Input/Output
D57#	B18	Source Synch	Input/Output
D58#	C21	Source Synch	Input/Output
D59#	B21	Source Synch	Input/Output
D60#	B19	Source Synch	Input/Output

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
D61#	A19	Source Synch	Input/Output
D62#	A22	Source Synch	Input/Output
D63#	B22	Source Synch	Input/Output
DBI0#	A8	Source Synch	Input/Output
DBI1#	G11	Source Synch	Input/Output
DBI2#	D19	Source Synch	Input/Output
DBI3#	C20	Source Synch	Input/Output
DBR#	AC2	Power/Other	Output
DBSY#	B2	Common Clock	Input/Output
DEFER#	G7	Common Clock	Input
DPRSTP#	T2	Asynch CMOS	Input
DPSLP#	P1	Asynch CMOS	Input
DRDY#	C1	Common Clock	Input/Output
DSTBN0#	C8	Source Synch	Input/Output
DSTBN1#	G12	Source Synch	Input/Output
DSTBN2#	G20	Source Synch	Input/Output
DSTBN3#	A16	Source Synch	Input/Output
DSTBP0#	B9	Source Synch	Input/Output
DSTBP1#	E12	Source Synch	Input/Output
DSTBP2#	G19	Source Synch	Input/Output
DSTBP3#	C17	Source Synch	Input/Output
FC0/ BOOTSELECT	Y1	Power/Other	
FC3	J2	Power/Other	
FC5	F2	Power/Other	
FC8	AK6	Power/Other	
FC10	E24	Power/Other	
FC15	H29	Power/Other	
FC18	AE3	Power/Other	
FC20	E5	Power/Other	
FC21	F6	Power/Other	
FC22	J3	Power/Other	
FC23	A24	Power/Other	
FC24	AK1	Power/Other	
FC25	AL1	Power/Other	
FC26	E29	Power/Other	
FC27	G1	Power/Other	
FC28	U1	Power/Other	
FC29	U2	Power/Other	
FC30	U3	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
FC31	J16	Power/Other	
FC32	H15	Power/Other	
FC33	H16	Power/Other	
FC34	J17	Power/Other	
FC35	H4	Power/Other	
FC36	AD3	Power/Other	
FC37	AB3	Power/Other	
FC38	G10	Power/Other	
FC39	AA2	Power/Other	
FC40	AM6	Power/Other	
FC41	C9	Power/Other	
FERR#/PBE#	R3	Asynch CMOS	Output
GTLREF0	H1	Power/Other	Input
GTLREF1	H2	Power/Other	Input
HIT#	D4	Common Clock	Input/Output
HITM#	E4	Common Clock	Input/Output
IERR#	AB2	Asynch CMOS	Output
IGNNE#	N2	Asynch CMOS	Input
INIT#	P3	Asynch CMOS	Input
ITP_CLK0	AK3	TAP	Input
ITP_CLK1	AJ3	TAP	Input
LINT0	K1	Asynch CMOS	Input
LINT1	L1	Asynch CMOS	Input
LOCK#	C3	Common Clock	Input/Output
MSID0	W1	Power/Other	Output
MSID1	V1	Power/Other	Output
PECI	G5	Power/Other	Input/Output
PROCHOT#	AL2	Asynch CMOS	Input/Output
PSI#	Y3	Asynch CMOS	Output
PWRGOOD	N1	Power/Other	Input
REQ0#	K4	Source Synch	Input/Output
REQ1#	J5	Source Synch	Input/Output
REQ2#	M6	Source Synch	Input/Output
REQ3#	K6	Source Synch	Input/Output
REQ4#	J6	Source Synch	Input/Output
RESERVED	V2		
RESERVED	A20		
RESERVED	AC4		
RESERVED	AE4		

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
RESERVED	AE6		
RESERVED	AH2		
RESERVED	D1		
RESERVED	D14		
RESERVED	D16		
RESERVED	E23		
RESERVED	E6		
RESERVED	E7		
RESERVED	F23		
RESERVED	F29		
RESERVED	G6		
RESERVED	N4		
RESERVED	N5		
RESERVED	P5		
RESET#	G23	Common Clock	Input
RS0#	B3	Common Clock	Input
RS1#	F5	Common Clock	Input
RS2#	A3	Common Clock	Input
SKTOCC#	AE8	Power/Other	Output
SLP#	L2	Asynch CMOS	Input
SMI#	P2	Asynch CMOS	Input
STPCLK#	M3	Asynch CMOS	Input
TCK	AE1	TAP	Input
TDI	AD1	TAP	Input
TDO	AF1	TAP	Output
TESTHI0	F26	Power/Other	Input
TESTHI1	W3	Power/Other	Input
TESTHI10	H5	Power/Other	Input
TESTHI12/ FC44	W2	Power/Other	Input
TESTHI2	F25	Power/Other	Input
TESTHI3	G25	Power/Other	Input
TESTHI4	G27	Power/Other	Input
TESTHI5	G26	Power/Other	Input
TESTHI6	G24	Power/Other	Input
TESTHI7	F24	Power/Other	Input
TESTHI8/FC42	G3	Power/Other	Input
TESTHI9/FC43	G4	Power/Other	Input
THERMTRIP#	M2	Asynch CMOS	Output
TMS	AC1	TAP	Input

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
TRDY#	E3	Common Clock	Input
TRST#	AG1	TAP	Input
VCC	AA8	Power/Other	
VCC	AB8	Power/Other	
VCC	AC23	Power/Other	
VCC	AC24	Power/Other	
VCC	AC25	Power/Other	
VCC	AC26	Power/Other	
VCC	AC27	Power/Other	
VCC	AC28	Power/Other	
VCC	AC29	Power/Other	
VCC	AC30	Power/Other	
VCC	AC8	Power/Other	
VCC	AD23	Power/Other	
VCC	AD24	Power/Other	
VCC	AD25	Power/Other	
VCC	AD26	Power/Other	
VCC	AD27	Power/Other	
VCC	AD28	Power/Other	
VCC	AD29	Power/Other	
VCC	AD30	Power/Other	
VCC	AD8	Power/Other	
VCC	AE11	Power/Other	
VCC	AE12	Power/Other	
VCC	AE14	Power/Other	
VCC	AE15	Power/Other	
VCC	AE18	Power/Other	
VCC	AE19	Power/Other	
VCC	AE21	Power/Other	
VCC	AE22	Power/Other	
VCC	AE23	Power/Other	
VCC	AE9	Power/Other	
VCC	AF11	Power/Other	
VCC	AF12	Power/Other	
VCC	AF14	Power/Other	
VCC	AF15	Power/Other	
VCC	AF18	Power/Other	
VCC	AF19	Power/Other	
VCC	AF21	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VCC	AF22	Power/Other	
VCC	AF8	Power/Other	
VCC	AF9	Power/Other	
VCC	AG11	Power/Other	
VCC	AG12	Power/Other	
VCC	AG14	Power/Other	
VCC	AG15	Power/Other	
VCC	AG18	Power/Other	
VCC	AG19	Power/Other	
VCC	AG21	Power/Other	
VCC	AG22	Power/Other	
VCC	AG25	Power/Other	
VCC	AG26	Power/Other	
VCC	AG27	Power/Other	
VCC	AG28	Power/Other	
VCC	AG29	Power/Other	
VCC	AG30	Power/Other	
VCC	AG8	Power/Other	
VCC	AG9	Power/Other	
VCC	AH11	Power/Other	
VCC	AH12	Power/Other	
VCC	AH14	Power/Other	
VCC	AH15	Power/Other	
VCC	AH18	Power/Other	
VCC	AH19	Power/Other	
VCC	AH21	Power/Other	
VCC	AH22	Power/Other	
VCC	AH25	Power/Other	
VCC	AH26	Power/Other	
VCC	AH27	Power/Other	
VCC	AH28	Power/Other	
VCC	AH29	Power/Other	
VCC	AH30	Power/Other	
VCC	AH8	Power/Other	
VCC	AH9	Power/Other	
VCC	AJ11	Power/Other	
VCC	AJ12	Power/Other	
VCC	AJ14	Power/Other	
VCC	AJ15	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VCC	AJ18	Power/Other	
VCC	AJ19	Power/Other	
VCC	AJ21	Power/Other	
VCC	AJ22	Power/Other	
VCC	AJ25	Power/Other	
VCC	AJ26	Power/Other	
VCC	AJ8	Power/Other	
VCC	AJ9	Power/Other	
VCC	AK11	Power/Other	
VCC	AK12	Power/Other	
VCC	AK14	Power/Other	
VCC	AK15	Power/Other	
VCC	AK18	Power/Other	
VCC	AK19	Power/Other	
VCC	AK21	Power/Other	
VCC	AK22	Power/Other	
VCC	AK25	Power/Other	
VCC	AK26	Power/Other	
VCC	AK8	Power/Other	
VCC	AK9	Power/Other	
VCC	AL11	Power/Other	
VCC	AL12	Power/Other	
VCC	AL14	Power/Other	
VCC	AL15	Power/Other	
VCC	AL18	Power/Other	
VCC	AL19	Power/Other	
VCC	AL21	Power/Other	
VCC	AL22	Power/Other	
VCC	AL25	Power/Other	
VCC	AL26	Power/Other	
VCC	AL29	Power/Other	
VCC	AL30	Power/Other	
VCC	AL8	Power/Other	
VCC	AL9	Power/Other	
VCC	AM11	Power/Other	
VCC	AM12	Power/Other	
VCC	AM14	Power/Other	
VCC	AM15	Power/Other	
VCC	AM18	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VCC	AM19	Power/Other	
VCC	AM21	Power/Other	
VCC	AM22	Power/Other	
VCC	AM25	Power/Other	
VCC	AM26	Power/Other	
VCC	AM29	Power/Other	
VCC	AM30	Power/Other	
VCC	AM8	Power/Other	
VCC	AM9	Power/Other	
VCC	AN11	Power/Other	
VCC	AN12	Power/Other	
VCC	AN14	Power/Other	
VCC	AN15	Power/Other	
VCC	AN18	Power/Other	
VCC	AN19	Power/Other	
VCC	AN21	Power/Other	
VCC	AN22	Power/Other	
VCC	AN25	Power/Other	
VCC	AN26	Power/Other	
VCC	AN29	Power/Other	
VCC	AN30	Power/Other	
VCC	AN8	Power/Other	
VCC	AN9	Power/Other	
VCC	J10	Power/Other	
VCC	J11	Power/Other	
VCC	J12	Power/Other	
VCC	J13	Power/Other	
VCC	J14	Power/Other	
VCC	J15	Power/Other	
VCC	J18	Power/Other	
VCC	J19	Power/Other	
VCC	J20	Power/Other	
VCC	J21	Power/Other	
VCC	J22	Power/Other	
VCC	J23	Power/Other	
VCC	J24	Power/Other	
VCC	J25	Power/Other	
VCC	J26	Power/Other	
VCC	J27	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VCC	J28	Power/Other	
VCC	J29	Power/Other	
VCC	J30	Power/Other	
VCC	J8	Power/Other	
VCC	J9	Power/Other	
VCC	K23	Power/Other	
VCC	K24	Power/Other	
VCC	K25	Power/Other	
VCC	K26	Power/Other	
VCC	K27	Power/Other	
VCC	K28	Power/Other	
VCC	K29	Power/Other	
VCC	K30	Power/Other	
VCC	K8	Power/Other	
VCC	L8	Power/Other	
VCC	M23	Power/Other	
VCC	M24	Power/Other	
VCC	M25	Power/Other	
VCC	M26	Power/Other	
VCC	M27	Power/Other	
VCC	M28	Power/Other	
VCC	M29	Power/Other	
VCC	M30	Power/Other	
VCC	M8	Power/Other	
VCC	N23	Power/Other	
VCC	N24	Power/Other	
VCC	N25	Power/Other	
VCC	N26	Power/Other	
VCC	N27	Power/Other	
VCC	N28	Power/Other	
VCC	N29	Power/Other	
VCC	N30	Power/Other	
VCC	N8	Power/Other	
VCC	P8	Power/Other	
VCC	R8	Power/Other	
VCC	T23	Power/Other	
VCC	T24	Power/Other	
VCC	T25	Power/Other	
VCC	T26	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VCC	T27	Power/Other	
VCC	T28	Power/Other	
VCC	T29	Power/Other	
VCC	T30	Power/Other	
VCC	T8	Power/Other	
VCC	U23	Power/Other	
VCC	U24	Power/Other	
VCC	U25	Power/Other	
VCC	U26	Power/Other	
VCC	U27	Power/Other	
VCC	U28	Power/Other	
VCC	U29	Power/Other	
VCC	U30	Power/Other	
VCC	U8	Power/Other	
VCC	V8	Power/Other	
VCC	W23	Power/Other	
VCC	W24	Power/Other	
VCC	W25	Power/Other	
VCC	W26	Power/Other	
VCC	W27	Power/Other	
VCC	W28	Power/Other	
VCC	W29	Power/Other	
VCC	W30	Power/Other	
VCC	W8	Power/Other	
VCC	Y23	Power/Other	
VCC	Y24	Power/Other	
VCC	Y25	Power/Other	
VCC	Y26	Power/Other	
VCC	Y27	Power/Other	
VCC	Y28	Power/Other	
VCC	Y29	Power/Other	
VCC	Y30	Power/Other	
VCC	Y8	Power/Other	
VCC_MB_REGULATION	AN5	Power/Other	Output
VCC_SENSE	AN3	Power/Other	Output
VCCA	A23	Power/Other	
VCCIOPLL	C23	Power/Other	
VCCPLL	D23	Power/Other	
VID_SELECT	AN7	Power/Other	Output

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VID0	AM2	Asynch CMOS	Output
VID1	AL5	Asynch CMOS	Output
VID2	AM3	Asynch CMOS	Output
VID3	AL6	Asynch CMOS	Output
VID4	AK4	Asynch CMOS	Output
VID5	AL4	Asynch CMOS	Output
VID6	AM5	Asynch CMOS	Output
VID7	AM7	Asynch CMOS	Output
VRDSEL	AL3	Power/Other	
VSS	B1	Power/Other	
VSS	B11	Power/Other	
VSS	B14	Power/Other	
VSS	B17	Power/Other	
VSS	B20	Power/Other	
VSS	B24	Power/Other	
VSS	B5	Power/Other	
VSS	B8	Power/Other	
VSS	A12	Power/Other	
VSS	A15	Power/Other	
VSS	A18	Power/Other	
VSS	A2	Power/Other	
VSS	A21	Power/Other	
VSS	A6	Power/Other	
VSS	A9	Power/Other	
VSS	AA23	Power/Other	
VSS	AA24	Power/Other	
VSS	AA25	Power/Other	
VSS	AA26	Power/Other	
VSS	AA27	Power/Other	
VSS	AA28	Power/Other	
VSS	AA29	Power/Other	
VSS	AA3	Power/Other	
VSS	AA30	Power/Other	
VSS	AA6	Power/Other	
VSS	AA7	Power/Other	
VSS	AB1	Power/Other	
VSS	AB23	Power/Other	
VSS	AB24	Power/Other	
VSS	AB25	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	AB26	Power/Other	
VSS	AB27	Power/Other	
VSS	AB28	Power/Other	
VSS	AB29	Power/Other	
VSS	AB30	Power/Other	
VSS	AB7	Power/Other	
VSS	AC3	Power/Other	
VSS	AC6	Power/Other	
VSS	AC7	Power/Other	
VSS	AD4	Power/Other	
VSS	AD7	Power/Other	
VSS	AE10	Power/Other	
VSS	AE13	Power/Other	
VSS	AE16	Power/Other	
VSS	AE17	Power/Other	
VSS	AE2	Power/Other	
VSS	AE20	Power/Other	
VSS	AE24	Power/Other	
VSS	AE25	Power/Other	
VSS	AE26	Power/Other	
VSS	AE27	Power/Other	
VSS	AE28	Power/Other	
VSS	AE29	Power/Other	
VSS	AE30	Power/Other	
VSS	AE5	Power/Other	
VSS	AE7	Power/Other	
VSS	AF10	Power/Other	
VSS	AF13	Power/Other	
VSS	AF16	Power/Other	
VSS	AF17	Power/Other	
VSS	AF20	Power/Other	
VSS	AF23	Power/Other	
VSS	AF24	Power/Other	
VSS	AF25	Power/Other	
VSS	AF26	Power/Other	
VSS	AF27	Power/Other	
VSS	AF28	Power/Other	
VSS	AF29	Power/Other	
VSS	AF3	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	AF30	Power/Other	
VSS	AF6	Power/Other	
VSS	AF7	Power/Other	
VSS	AG10	Power/Other	
VSS	AG13	Power/Other	
VSS	AG16	Power/Other	
VSS	AG17	Power/Other	
VSS	AG20	Power/Other	
VSS	AG23	Power/Other	
VSS	AG24	Power/Other	
VSS	AG7	Power/Other	
VSS	AH1	Power/Other	
VSS	AH10	Power/Other	
VSS	AH13	Power/Other	
VSS	AH16	Power/Other	
VSS	AH17	Power/Other	
VSS	AH20	Power/Other	
VSS	AH23	Power/Other	
VSS	AH24	Power/Other	
VSS	AH3	Power/Other	
VSS	AH6	Power/Other	
VSS	AH7	Power/Other	
VSS	AJ10	Power/Other	
VSS	AJ13	Power/Other	
VSS	AJ16	Power/Other	
VSS	AJ17	Power/Other	
VSS	AJ20	Power/Other	
VSS	AJ23	Power/Other	
VSS	AJ24	Power/Other	
VSS	AJ27	Power/Other	
VSS	AJ28	Power/Other	
VSS	AJ29	Power/Other	
VSS	AJ30	Power/Other	
VSS	AJ4	Power/Other	
VSS	AJ7	Power/Other	
VSS	AK10	Power/Other	
VSS	AK13	Power/Other	
VSS	AK16	Power/Other	
VSS	AK17	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	AK2	Power/Other	
VSS	AK20	Power/Other	
VSS	AK23	Power/Other	
VSS	AK24	Power/Other	
VSS	AK27	Power/Other	
VSS	AK28	Power/Other	
VSS	AK29	Power/Other	
VSS	AK30	Power/Other	
VSS	AK5	Power/Other	
VSS	AK7	Power/Other	
VSS	AL10	Power/Other	
VSS	AL13	Power/Other	
VSS	AL16	Power/Other	
VSS	AL17	Power/Other	
VSS	AL20	Power/Other	
VSS	AL23	Power/Other	
VSS	AL24	Power/Other	
VSS	AL27	Power/Other	
VSS	AL28	Power/Other	
VSS	AL7	Power/Other	
VSS	AM1	Power/Other	
VSS	AM10	Power/Other	
VSS	AM13	Power/Other	
VSS	AM16	Power/Other	
VSS	AM17	Power/Other	
VSS	AM20	Power/Other	
VSS	AM23	Power/Other	
VSS	AM24	Power/Other	
VSS	AM27	Power/Other	
VSS	AM28	Power/Other	
VSS	AM4	Power/Other	
VSS	AN1	Power/Other	
VSS	AN10	Power/Other	
VSS	AN13	Power/Other	
VSS	AN16	Power/Other	
VSS	AN17	Power/Other	
VSS	AN2	Power/Other	
VSS	AN20	Power/Other	
VSS	AN23	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	AN24	Power/Other	
VSS	AN27	Power/Other	
VSS	AN28	Power/Other	
VSS	C10	Power/Other	
VSS	C13	Power/Other	
VSS	C16	Power/Other	
VSS	C19	Power/Other	
VSS	C22	Power/Other	
VSS	C24	Power/Other	
VSS	C4	Power/Other	
VSS	C7	Power/Other	
VSS	D12	Power/Other	
VSS	D15	Power/Other	
VSS	D18	Power/Other	
VSS	D21	Power/Other	
VSS	D24	Power/Other	
VSS	D3	Power/Other	
VSS	D5	Power/Other	
VSS	D6	Power/Other	
VSS	D9	Power/Other	
VSS	E11	Power/Other	
VSS	E14	Power/Other	
VSS	E17	Power/Other	
VSS	E2	Power/Other	
VSS	E20	Power/Other	
VSS	E25	Power/Other	
VSS	E26	Power/Other	
VSS	E27	Power/Other	
VSS	E28	Power/Other	
VSS	E8	Power/Other	
VSS	F10	Power/Other	
VSS	F13	Power/Other	
VSS	F16	Power/Other	
VSS	F19	Power/Other	
VSS	F22	Power/Other	
VSS	F4	Power/Other	
VSS	F7	Power/Other	
VSS	H10	Power/Other	
VSS	H11	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	H12	Power/Other	
VSS	H13	Power/Other	
VSS	H14	Power/Other	
VSS	H17	Power/Other	
VSS	H18	Power/Other	
VSS	H19	Power/Other	
VSS	H20	Power/Other	
VSS	H21	Power/Other	
VSS	H22	Power/Other	
VSS	H23	Power/Other	
VSS	H24	Power/Other	
VSS	H25	Power/Other	
VSS	H26	Power/Other	
VSS	H27	Power/Other	
VSS	H28	Power/Other	
VSS	H3	Power/Other	
VSS	H6	Power/Other	
VSS	H7	Power/Other	
VSS	H8	Power/Other	
VSS	H9	Power/Other	
VSS	J4	Power/Other	
VSS	J7	Power/Other	
VSS	K2	Power/Other	
VSS	K5	Power/Other	
VSS	K7	Power/Other	
VSS	L23	Power/Other	
VSS	L24	Power/Other	
VSS	L25	Power/Other	
VSS	L26	Power/Other	
VSS	L27	Power/Other	
VSS	L28	Power/Other	
VSS	L29	Power/Other	
VSS	L3	Power/Other	
VSS	L30	Power/Other	
VSS	L6	Power/Other	
VSS	L7	Power/Other	
VSS	M1	Power/Other	
VSS	M7	Power/Other	
VSS	N3	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	N6	Power/Other	
VSS	N7	Power/Other	
VSS	P23	Power/Other	
VSS	P24	Power/Other	
VSS	P25	Power/Other	
VSS	P26	Power/Other	
VSS	P27	Power/Other	
VSS	P28	Power/Other	
VSS	P29	Power/Other	
VSS	P30	Power/Other	
VSS	P4	Power/Other	
VSS	P7	Power/Other	
VSS	R2	Power/Other	
VSS	R23	Power/Other	
VSS	R24	Power/Other	
VSS	R25	Power/Other	
VSS	R26	Power/Other	
VSS	R27	Power/Other	
VSS	R28	Power/Other	
VSS	R29	Power/Other	
VSS	R30	Power/Other	
VSS	R5	Power/Other	
VSS	R7	Power/Other	
VSS	T3	Power/Other	
VSS	T6	Power/Other	
VSS	T7	Power/Other	
VSS	U7	Power/Other	
VSS	V23	Power/Other	
VSS	V24	Power/Other	
VSS	V25	Power/Other	
VSS	V26	Power/Other	
VSS	V27	Power/Other	
VSS	V28	Power/Other	
VSS	V29	Power/Other	
VSS	V3	Power/Other	
VSS	V30	Power/Other	
VSS	V6	Power/Other	
VSS	V7	Power/Other	
VSS	W4	Power/Other	

Table 22. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	W7	Power/Other	
VSS	Y2	Power/Other	
VSS	Y5	Power/Other	
VSS	Y7	Power/Other	
VSS_MB_REGULATION	AN6	Power/Other	Output
VSS_SENSE	AN4	Power/Other	Output
VSSA	B23	Power/Other	
VTT	B25	Power/Other	
VTT	B26	Power/Other	
VTT	B27	Power/Other	
VTT	B28	Power/Other	
VTT	B29	Power/Other	
VTT	B30	Power/Other	
VTT	A25	Power/Other	
VTT	A26	Power/Other	
VTT	A27	Power/Other	
VTT	A28	Power/Other	
VTT	A29	Power/Other	
VTT	A30	Power/Other	
VTT	C25	Power/Other	
VTT	C26	Power/Other	
VTT	C27	Power/Other	
VTT	C28	Power/Other	
VTT	C29	Power/Other	
VTT	C30	Power/Other	
VTT	D25	Power/Other	
VTT	D26	Power/Other	
VTT	D27	Power/Other	
VTT	D28	Power/Other	
VTT	D29	Power/Other	
VTT	D30	Power/Other	
VTT_OUT_LEFT	J1	Power/Other	Output
VTT_OUT_RIGHT	AA1	Power/Other	Output
VTT_SEL	F27	Power/Other	Output

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
A2	VSS	Power/Other	
A3	RS2#	Common Clock	Input
A4	D02#	Source Synch	Input/Output
A5	D04#	Source Synch	Input/Output
A6	VSS	Power/Other	
A7	D07#	Source Synch	Input/Output
A8	DBI0#	Source Synch	Input/Output
A9	VSS	Power/Other	
A10	D08#	Source Synch	Input/Output
A11	D09#	Source Synch	Input/Output
A12	VSS	Power/Other	
A13	COMP0	Power/Other	Input
A14	D50#	Source Synch	Input/Output
A15	VSS	Power/Other	
A16	DSTBN3#	Source Synch	Input/Output
A17	D56#	Source Synch	Input/Output
A18	VSS	Power/Other	
A19	D61#	Source Synch	Input/Output
A20	RESERVED		
A21	VSS	Power/Other	
A22	D62#	Source Synch	Input/Output
A23	VCCA	Power/Other	
A24	FC23	Power/Other	
A25	VTT	Power/Other	
A26	VTT	Power/Other	
A27	VTT	Power/Other	
A28	VTT	Power/Other	
A29	VTT	Power/Other	
A30	VTT	Power/Other	
B1	VSS	Power/Other	
B2	DBSY#	Common Clock	Input/Output
B3	RS0#	Common Clock	Input
B4	D00#	Source Synch	Input/Output
B5	VSS	Power/Other	
B6	D05#	Source Synch	Input/Output
B7	D06#	Source Synch	Input/Output
B8	VSS	Power/Other	
B9	DSTBP0#	Source Synch	Input/Output
B10	D10#	Source Synch	Input/Output

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
B11	VSS	Power/Other	
B12	D13#	Source Synch	Input/Output
B13	COMP8	Power/Other	Input
B14	VSS	Power/Other	
B15	D53#	Source Synch	Input/Output
B16	D55#	Source Synch	Input/Output
B17	VSS	Power/Other	
B18	D57#	Source Synch	Input/Output
B19	D60#	Source Synch	Input/Output
B20	VSS	Power/Other	
B21	D59#	Source Synch	Input/Output
B22	D63#	Source Synch	Input/Output
B23	VSSA	Power/Other	
B24	VSS	Power/Other	
B25	VTT	Power/Other	
B26	VTT	Power/Other	
B27	VTT	Power/Other	
B28	VTT	Power/Other	
B29	VTT	Power/Other	
B30	VTT	Power/Other	
C1	DRDY#	Common Clock	Input/Output
C2	BNR#	Common Clock	Input/Output
C3	LOCK#	Common Clock	Input/Output
C4	VSS	Power/Other	
C5	D01#	Source Synch	Input/Output
C6	D03#	Source Synch	Input/Output
C7	VSS	Power/Other	
C8	DSTBN0#	Source Synch	Input/Output
C9	FC41	Power/Other	
C10	VSS	Power/Other	
C11	D11#	Source Synch	Input/Output
C12	D14#	Source Synch	Input/Output
C13	VSS	Power/Other	
C14	D52#	Source Synch	Input/Output
C15	D51#	Source Synch	Input/Output
C16	VSS	Power/Other	
C17	DSTBP3#	Source Synch	Input/Output
C18	D54#	Source Synch	Input/Output
C19	VSS	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
C20	DBI3#	Source Synch	Input/Output
C21	D58#	Source Synch	Input/Output
C22	VSS	Power/Other	
C23	VCCIOPLL	Power/Other	
C24	VSS	Power/Other	
C25	VTT	Power/Other	
C26	VTT	Power/Other	
C27	VTT	Power/Other	
C28	VTT	Power/Other	
C29	VTT	Power/Other	
C30	VTT	Power/Other	
D1	RESERVED		
D2	ADS#	Common Clock	Input/Output
D3	VSS	Power/Other	
D4	HIT#	Common Clock	Input/Output
D5	VSS	Power/Other	
D6	VSS	Power/Other	
D7	D20#	Source Synch	Input/Output
D8	D12#	Source Synch	Input/Output
D9	VSS	Power/Other	
D10	D22#	Source Synch	Input/Output
D11	D15#	Source Synch	Input/Output
D12	VSS	Power/Other	
D13	D25#	Source Synch	Input/Output
D14	RESERVED		
D15	VSS	Power/Other	
D16	RESERVED		
D17	D49#	Source Synch	Input/Output
D18	VSS	Power/Other	
D19	DBI2#	Source Synch	Input/Output
D20	D48#	Source Synch	Input/Output
D21	VSS	Power/Other	
D22	D46#	Source Synch	Input/Output
D23	VCCPLL	Power/Other	
D24	VSS	Power/Other	
D25	VTT	Power/Other	
D26	VTT	Power/Other	
D27	VTT	Power/Other	
D28	VTT	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
D29	VTT	Power/Other	
D30	VTT	Power/Other	
E2	VSS	Power/Other	
E3	TRDY#	Common Clock	Input
E4	HITM#	Common Clock	Input/Output
E5	FC20	Power/Other	
E6	RESERVED		
E7	RESERVED		
E8	VSS	Power/Other	
E9	D19#	Source Synch	Input/Output
E10	D21#	Source Synch	Input/Output
E11	VSS	Power/Other	
E12	DSTBP1#	Source Synch	Input/Output
E13	D26#	Source Synch	Input/Output
E14	VSS	Power/Other	
E15	D33#	Source Synch	Input/Output
E16	D34#	Source Synch	Input/Output
E17	VSS	Power/Other	
E18	D39#	Source Synch	Input/Output
E19	D40#	Source Synch	Input/Output
E20	VSS	Power/Other	
E21	D42#	Source Synch	Input/Output
E22	D45#	Source Synch	Input/Output
E23	RESERVED		
E24	FC10	Power/Other	
E25	VSS	Power/Other	
E26	VSS	Power/Other	
E27	VSS	Power/Other	
E28	VSS	Power/Other	
E29	FC26	Power/Other	
F2	FC5	Power/Other	
F3	BR0#	Common Clock	Input/Output
F4	VSS	Power/Other	
F5	RS1#	Common Clock	Input
F6	FC21	Power/Other	
F7	VSS	Power/Other	
F8	D17#	Source Synch	Input/Output
F9	D18#	Source Synch	Input/Output
F10	VSS	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
F11	D23#	Source Synch	Input/Output
F12	D24#	Source Synch	Input/Output
F13	VSS	Power/Other	
F14	D28#	Source Synch	Input/Output
F15	D30#	Source Synch	Input/Output
F16	VSS	Power/Other	
F17	D37#	Source Synch	Input/Output
F18	D38#	Source Synch	Input/Output
F19	VSS	Power/Other	
F20	D41#	Source Synch	Input/Output
F21	D43#	Source Synch	Input/Output
F22	VSS	Power/Other	
F23	RESERVED		
F24	TESTHI7	Power/Other	Input
F25	TESTHI2	Power/Other	Input
F26	TESTHI0	Power/Other	Input
F27	VTT_SEL	Power/Other	Output
F28	BCLK0	Clock	Input
F29	RESERVED		
G1	FC27	Power/Other	
G2	COMP2	Power/Other	Input
G3	TESTHI8/ FC42	Power/Other	Input
G4	TESTHI9/ FC43	Power/Other	Input
G5	PECI	Power/Other	Input/Output
G6	RESERVED		
G7	DEFER#	Common Clock	Input
G8	BPRI#	Common Clock	Input
G9	D16#	Source Synch	Input/Output
G10	FC38	Power/Other	
G11	DBI1#	Source Synch	Input/Output
G12	DSTBN1#	Source Synch	Input/Output
G13	D27#	Source Synch	Input/Output
G14	D29#	Source Synch	Input/Output
G15	D31#	Source Synch	Input/Output
G16	D32#	Source Synch	Input/Output
G17	D36#	Source Synch	Input/Output
G18	D35#	Source Synch	Input/Output
G19	DSTBP2#	Source Synch	Input/Output

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
G20	DSTBN2#	Source Synch	Input/Output
G21	D44#	Source Synch	Input/Output
G22	D47#	Source Synch	Input/Output
G23	RESET#	Common Clock	Input
G24	TESTHI6	Power/Other	Input
G25	TESTHI3	Power/Other	Input
G26	TESTHI5	Power/Other	Input
G27	TESTHI4	Power/Other	Input
G28	BCLK1	Clock	Input
G29	BSEL0	Asynch CMOS	Output
G30	BSEL2	Asynch CMOS	Output
H1	GTLREF0	Power/Other	Input
H2	GTLREF1	Power/Other	Input
H3	VSS	Power/Other	
H4	FC35	Power/Other	
H5	TESTHI10	Power/Other	Input
H6	VSS	Power/Other	
H7	VSS	Power/Other	
H8	VSS	Power/Other	
H9	VSS	Power/Other	
H10	VSS	Power/Other	
H11	VSS	Power/Other	
H12	VSS	Power/Other	
H13	VSS	Power/Other	
H14	VSS	Power/Other	
H15	FC32	Power/Other	
H16	FC33	Power/Other	
H17	VSS	Power/Other	
H18	VSS	Power/Other	
H19	VSS	Power/Other	
H20	VSS	Power/Other	
H21	VSS	Power/Other	
H22	VSS	Power/Other	
H23	VSS	Power/Other	
H24	VSS	Power/Other	
H25	VSS	Power/Other	
H26	VSS	Power/Other	
H27	VSS	Power/Other	
H28	VSS	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
H29	FC15	Power/Other	
H30	BSEL1	Asynch CMOS	Output
J1	VTT_OUT_LEFT	Power/Other	Output
J2	FC3	Power/Other	
J3	FC22	Power/Other	
J4	VSS	Power/Other	
J5	REQ1#	Source Synch	Input/Output
J6	REQ4#	Source Synch	Input/Output
J7	VSS	Power/Other	
J8	VCC	Power/Other	
J9	VCC	Power/Other	
J10	VCC	Power/Other	
J11	VCC	Power/Other	
J12	VCC	Power/Other	
J13	VCC	Power/Other	
J14	VCC	Power/Other	
J15	VCC	Power/Other	
J16	FC31	Power/Other	
J17	FC34	Power/Other	
J18	VCC	Power/Other	
J19	VCC	Power/Other	
J20	VCC	Power/Other	
J21	VCC	Power/Other	
J22	VCC	Power/Other	
J23	VCC	Power/Other	
J24	VCC	Power/Other	
J25	VCC	Power/Other	
J26	VCC	Power/Other	
J27	VCC	Power/Other	
J28	VCC	Power/Other	
J29	VCC	Power/Other	
J30	VCC	Power/Other	
K1	LINT0	Asynch CMOS	Input
K2	VSS	Power/Other	
K3	A20M#	Asynch CMOS	Input
K4	REQ0#	Source Synch	Input/Output
K5	VSS	Power/Other	
K6	REQ3#	Source Synch	Input/Output
K7	VSS	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
K8	VCC	Power/Other	
K23	VCC	Power/Other	
K24	VCC	Power/Other	
K25	VCC	Power/Other	
K26	VCC	Power/Other	
K27	VCC	Power/Other	
K28	VCC	Power/Other	
K29	VCC	Power/Other	
K30	VCC	Power/Other	
L1	LINT1	Asynch CMOS	Input
L2	SLP#	Asynch CMOS	Input
L3	VSS	Power/Other	
L4	A06#	Source Synch	Input/Output
L5	A03#	Source Synch	Input/Output
L6	VSS	Power/Other	
L7	VSS	Power/Other	
L8	VCC	Power/Other	
L23	VSS	Power/Other	
L24	VSS	Power/Other	
L25	VSS	Power/Other	
L26	VSS	Power/Other	
L27	VSS	Power/Other	
L28	VSS	Power/Other	
L29	VSS	Power/Other	
L30	VSS	Power/Other	
M1	VSS	Power/Other	
M2	THERMTRIP#	Asynch CMOS	Output
M3	STPCLK#	Asynch CMOS	Input
M4	A07#	Source Synch	Input/Output
M5	A05#	Source Synch	Input/Output
M6	REQ2#	Source Synch	Input/Output
M7	VSS	Power/Other	
M8	VCC	Power/Other	
M23	VCC	Power/Other	
M24	VCC	Power/Other	
M25	VCC	Power/Other	
M26	VCC	Power/Other	
M27	VCC	Power/Other	
M28	VCC	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
M29	VCC	Power/Other	
M30	VCC	Power/Other	
N1	PWRGOOD	Power/Other	Input
N2	IGNNE#	Asynch CMOS	Input
N3	VSS	Power/Other	
N4	RESERVED		
N5	RESERVED		
N6	VSS	Power/Other	
N7	VSS	Power/Other	
N8	VCC	Power/Other	
N23	VCC	Power/Other	
N24	VCC	Power/Other	
N25	VCC	Power/Other	
N26	VCC	Power/Other	
N27	VCC	Power/Other	
N28	VCC	Power/Other	
N29	VCC	Power/Other	
N30	VCC	Power/Other	
P1	DPSLP#	Asynch CMOS	Input
P2	SMI#	Asynch CMOS	Input
P3	INIT#	Asynch CMOS	Input
P4	VSS	Power/Other	
P5	RESERVED		
P6	A04#	Source Synch	Input/Output
P7	VSS	Power/Other	
P8	VCC	Power/Other	
P23	VSS	Power/Other	
P24	VSS	Power/Other	
P25	VSS	Power/Other	
P26	VSS	Power/Other	
P27	VSS	Power/Other	
P28	VSS	Power/Other	
P29	VSS	Power/Other	
P30	VSS	Power/Other	
R1	COMP3	Power/Other	Input
R2	VSS	Power/Other	
R3	FERR#/PBE#	Asynch CMOS	Output
R4	A08#	Source Synch	Input/Output
R5	VSS	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
R6	ADSTB0#	Source Synch	Input/Output
R7	VSS	Power/Other	
R8	VCC	Power/Other	
R23	VSS	Power/Other	
R24	VSS	Power/Other	
R25	VSS	Power/Other	
R26	VSS	Power/Other	
R27	VSS	Power/Other	
R28	VSS	Power/Other	
R29	VSS	Power/Other	
R30	VSS	Power/Other	
T1	COMP1	Power/Other	Input
T2	DPRSTP#	Asynch CMOS	Input
T3	VSS	Power/Other	
T4	A11#	Source Synch	Input/Output
T5	A09#	Source Synch	Input/Output
T6	VSS	Power/Other	
T7	VSS	Power/Other	
T8	VCC	Power/Other	
T23	VCC	Power/Other	
T24	VCC	Power/Other	
T25	VCC	Power/Other	
T26	VCC	Power/Other	
T27	VCC	Power/Other	
T28	VCC	Power/Other	
T29	VCC	Power/Other	
T30	VCC	Power/Other	
U1	FC28	Power/Other	
U2	FC29	Power/Other	
U3	FC30	Power/Other	
U4	A13#	Source Synch	Input/Output
U5	A12#	Source Synch	Input/Output
U6	A10#	Source Synch	Input/Output
U7	VSS	Power/Other	
U8	VCC	Power/Other	
U23	VCC	Power/Other	
U24	VCC	Power/Other	
U25	VCC	Power/Other	
U26	VCC	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
U27	VCC	Power/Other	
U28	VCC	Power/Other	
U29	VCC	Power/Other	
U30	VCC	Power/Other	
V1	MSID1	Power/Other	Output
V2	RESERVED		
V3	VSS	Power/Other	
V4	A15#	Source Synch	Input/Output
V5	A14#	Source Synch	Input/Output
V6	VSS	Power/Other	
V7	VSS	Power/Other	
V8	VCC	Power/Other	
V23	VSS	Power/Other	
V24	VSS	Power/Other	
V25	VSS	Power/Other	
V26	VSS	Power/Other	
V27	VSS	Power/Other	
V28	VSS	Power/Other	
V29	VSS	Power/Other	
V30	VSS	Power/Other	
W1	MSID0	Power/Other	Output
W2	TESTHI12/ FC44	Power/Other	Input
W3	TESTHI1	Power/Other	Input
W4	VSS	Power/Other	
W5	A16#	Source Synch	Input/Output
W6	A18#	Source Synch	Input/Output
W7	VSS	Power/Other	
W8	VCC	Power/Other	
W23	VCC	Power/Other	
W24	VCC	Power/Other	
W25	VCC	Power/Other	
W26	VCC	Power/Other	
W27	VCC	Power/Other	
W28	VCC	Power/Other	
W29	VCC	Power/Other	
W30	VCC	Power/Other	
Y1	FC0/ BOOTSELECT	Power/Other	
Y2	VSS	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
Y3	PSI#	Asynch CMOS	Output
Y4	A20#	Source Synch	Input/Output
Y5	VSS	Power/Other	
Y6	A19#	Source Synch	Input/Output
Y7	VSS	Power/Other	
Y8	VCC	Power/Other	
Y23	VCC	Power/Other	
Y24	VCC	Power/Other	
Y25	VCC	Power/Other	
Y26	VCC	Power/Other	
Y27	VCC	Power/Other	
Y28	VCC	Power/Other	
Y29	VCC	Power/Other	
Y30	VCC	Power/Other	
AA1	VTT_OUT_RIGHT	Power/Other	Output
AA2	FC39	Power/Other	
AA3	VSS	Power/Other	
AA4	A21#	Source Synch	Input/Output
AA5	A23#	Source Synch	Input/Output
AA6	VSS	Power/Other	
AA7	VSS	Power/Other	
AA8	VCC	Power/Other	
AA23	VSS	Power/Other	
AA24	VSS	Power/Other	
AA25	VSS	Power/Other	
AA26	VSS	Power/Other	
AA27	VSS	Power/Other	
AA28	VSS	Power/Other	
AA29	VSS	Power/Other	
AA30	VSS	Power/Other	
AB1	VSS	Power/Other	
AB2	IERR#	Asynch CMOS	Output
AB3	FC37	Power/Other	
AB4	A26#	Source Synch	Input/Output
AB5	A24#	Source Synch	Input/Output
AB6	A17#	Source Synch	Input/Output
AB7	VSS	Power/Other	
AB8	VCC	Power/Other	
AB23	VSS	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AB24	VSS	Power/Other	
AB25	VSS	Power/Other	
AB26	VSS	Power/Other	
AB27	VSS	Power/Other	
AB28	VSS	Power/Other	
AB29	VSS	Power/Other	
AB30	VSS	Power/Other	
AC1	TMS	TAP	Input
AC2	DBR#	Power/Other	Output
AC3	VSS	Power/Other	
AC4	RESERVED		
AC5	A25#	Source Synch	Input/Output
AC6	VSS	Power/Other	
AC7	VSS	Power/Other	
AC8	VCC	Power/Other	
AC23	VCC	Power/Other	
AC24	VCC	Power/Other	
AC25	VCC	Power/Other	
AC26	VCC	Power/Other	
AC27	VCC	Power/Other	
AC28	VCC	Power/Other	
AC29	VCC	Power/Other	
AC30	VCC	Power/Other	
AD1	TDI	TAP	Input
AD2	BPM2#	Common Clock	Input/Output
AD3	FC36	Power/Other	
AD4	VSS	Power/Other	
AD5	ADSTB1#	Source Synch	Input/Output
AD6	A22#	Source Synch	Input/Output
AD7	VSS	Power/Other	
AD8	VCC	Power/Other	
AD23	VCC	Power/Other	
AD24	VCC	Power/Other	
AD25	VCC	Power/Other	
AD26	VCC	Power/Other	
AD27	VCC	Power/Other	
AD28	VCC	Power/Other	
AD29	VCC	Power/Other	
AD30	VCC	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AE1	TCK	TAP	Input
AE2	VSS	Power/Other	
AE3	FC18	Power/Other	
AE4	RESERVED		
AE5	VSS	Power/Other	
AE6	RESERVED		
AE7	VSS	Power/Other	
AE8	SKTOCC#	Power/Other	Output
AE9	VCC	Power/Other	
AE10	VSS	Power/Other	
AE11	VCC	Power/Other	
AE12	VCC	Power/Other	
AE13	VSS	Power/Other	
AE14	VCC	Power/Other	
AE15	VCC	Power/Other	
AE16	VSS	Power/Other	
AE17	VSS	Power/Other	
AE18	VCC	Power/Other	
AE19	VCC	Power/Other	
AE20	VSS	Power/Other	
AE21	VCC	Power/Other	
AE22	VCC	Power/Other	
AE23	VCC	Power/Other	
AE24	VSS	Power/Other	
AE25	VSS	Power/Other	
AE26	VSS	Power/Other	
AE27	VSS	Power/Other	
AE28	VSS	Power/Other	
AE29	VSS	Power/Other	
AE30	VSS	Power/Other	
AF1	TDO	TAP	Output
AF2	BPM4#	Common Clock	Input/Output
AF3	VSS	Power/Other	
AF4	A28#	Source Synch	Input/Output
AF5	A27#	Source Synch	Input/Output
AF6	VSS	Power/Other	
AF7	VSS	Power/Other	
AF8	VCC	Power/Other	
AF9	VCC	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AF10	VSS	Power/Other	
AF11	VCC	Power/Other	
AF12	VCC	Power/Other	
AF13	VSS	Power/Other	
AF14	VCC	Power/Other	
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VSS	Power/Other	
AF18	VCC	Power/Other	
AF19	VCC	Power/Other	
AF20	VSS	Power/Other	
AF21	VCC	Power/Other	
AF22	VCC	Power/Other	
AF23	VSS	Power/Other	
AF24	VSS	Power/Other	
AF25	VSS	Power/Other	
AF26	VSS	Power/Other	
AF27	VSS	Power/Other	
AF28	VSS	Power/Other	
AF29	VSS	Power/Other	
AF30	VSS	Power/Other	
AG1	TRST#	TAP	Input
AG2	BPM3#	Common Clock	Input/Output
AG3	BPM5#	Common Clock	Input/Output
AG4	A30#	Source Synch	Input/Output
AG5	A31#	Source Synch	Input/Output
AG6	A29#	Source Synch	Input/Output
AG7	VSS	Power/Other	
AG8	VCC	Power/Other	
AG9	VCC	Power/Other	
AG10	VSS	Power/Other	
AG11	VCC	Power/Other	
AG12	VCC	Power/Other	
AG13	VSS	Power/Other	
AG14	VCC	Power/Other	
AG15	VCC	Power/Other	
AG16	VSS	Power/Other	
AG17	VSS	Power/Other	
AG18	VCC	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AG19	VCC	Power/Other	
AG20	VSS	Power/Other	
AG21	VCC	Power/Other	
AG22	VCC	Power/Other	
AG23	VSS	Power/Other	
AG24	VSS	Power/Other	
AG25	VCC	Power/Other	
AG26	VCC	Power/Other	
AG27	VCC	Power/Other	
AG28	VCC	Power/Other	
AG29	VCC	Power/Other	
AG30	VCC	Power/Other	
AH1	VSS	Power/Other	
AH2	RESERVED		
AH3	VSS	Power/Other	
AH4	A32#	Source Synch	Input/Output
AH5	A33#	Source Synch	Input/Output
AH6	VSS	Power/Other	
AH7	VSS	Power/Other	
AH8	VCC	Power/Other	
AH9	VCC	Power/Other	
AH10	VSS	Power/Other	
AH11	VCC	Power/Other	
AH12	VCC	Power/Other	
AH13	VSS	Power/Other	
AH14	VCC	Power/Other	
AH15	VCC	Power/Other	
AH16	VSS	Power/Other	
AH17	VSS	Power/Other	
AH18	VCC	Power/Other	
AH19	VCC	Power/Other	
AH20	VSS	Power/Other	
AH21	VCC	Power/Other	
AH22	VCC	Power/Other	
AH23	VSS	Power/Other	
AH24	VSS	Power/Other	
AH25	VCC	Power/Other	
AH26	VCC	Power/Other	
AH27	VCC	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AH28	VCC	Power/Other	
AH29	VCC	Power/Other	
AH30	VCC	Power/Other	
AJ1	BPM1#	Common Clock	Input/Output
AJ2	BPM0#	Common Clock	Input/Output
AJ3	ITP_CLK1	TAP	Input
AJ4	VSS	Power/Other	
AJ5	A34#	Source Synch	Input/Output
AJ6	A35#	Source Synch	Input/Output
AJ7	VSS	Power/Other	
AJ8	VCC	Power/Other	
AJ9	VCC	Power/Other	
AJ10	VSS	Power/Other	
AJ11	VCC	Power/Other	
AJ12	VCC	Power/Other	
AJ13	VSS	Power/Other	
AJ14	VCC	Power/Other	
AJ15	VCC	Power/Other	
AJ16	VSS	Power/Other	
AJ17	VSS	Power/Other	
AJ18	VCC	Power/Other	
AJ19	VCC	Power/Other	
AJ20	VSS	Power/Other	
AJ21	VCC	Power/Other	
AJ22	VCC	Power/Other	
AJ23	VSS	Power/Other	
AJ24	VSS	Power/Other	
AJ25	VCC	Power/Other	
AJ26	VCC	Power/Other	
AJ27	VSS	Power/Other	
AJ28	VSS	Power/Other	
AJ29	VSS	Power/Other	
AJ30	VSS	Power/Other	
AK1	FC24	Power/Other	
AK2	VSS	Power/Other	
AK3	ITP_CLK0	TAP	Input
AK4	VID4	Asynch CMOS	Output
AK5	VSS	Power/Other	
AK6	FC8	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AK7	VSS	Power/Other	
AK8	VCC	Power/Other	
AK9	VCC	Power/Other	
AK10	VSS	Power/Other	
AK11	VCC	Power/Other	
AK12	VCC	Power/Other	
AK13	VSS	Power/Other	
AK14	VCC	Power/Other	
AK15	VCC	Power/Other	
AK16	VSS	Power/Other	
AK17	VSS	Power/Other	
AK18	VCC	Power/Other	
AK19	VCC	Power/Other	
AK20	VSS	Power/Other	
AK21	VCC	Power/Other	
AK22	VCC	Power/Other	
AK23	VSS	Power/Other	
AK24	VSS	Power/Other	
AK25	VCC	Power/Other	
AK26	VCC	Power/Other	
AK27	VSS	Power/Other	
AK28	VSS	Power/Other	
AK29	VSS	Power/Other	
AK30	VSS	Power/Other	
AL1	FC25	Power/Other	
AL2	PROCHOT#	Asynch CMOS	Input/Output
AL3	VRDSEL	Power/Other	
AL4	VID5	Asynch CMOS	Output
AL5	VID1	Asynch CMOS	Output
AL6	VID3	Asynch CMOS	Output
AL7	VSS	Power/Other	
AL8	VCC	Power/Other	
AL9	VCC	Power/Other	
AL10	VSS	Power/Other	
AL11	VCC	Power/Other	
AL12	VCC	Power/Other	
AL13	VSS	Power/Other	
AL14	VCC	Power/Other	
AL15	VCC	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AL16	VSS	Power/Other	
AL17	VSS	Power/Other	
AL18	VCC	Power/Other	
AL19	VCC	Power/Other	
AL20	VSS	Power/Other	
AL21	VCC	Power/Other	
AL22	VCC	Power/Other	
AL23	VSS	Power/Other	
AL24	VSS	Power/Other	
AL25	VCC	Power/Other	
AL26	VCC	Power/Other	
AL27	VSS	Power/Other	
AL28	VSS	Power/Other	
AL29	VCC	Power/Other	
AL30	VCC	Power/Other	
AM1	VSS	Power/Other	
AM10	VSS	Power/Other	
AM11	VCC	Power/Other	
AM12	VCC	Power/Other	
AM13	VSS	Power/Other	
AM14	VCC	Power/Other	
AM15	VCC	Power/Other	
AM16	VSS	Power/Other	
AM17	VSS	Power/Other	
AM18	VCC	Power/Other	
AM19	VCC	Power/Other	
AM2	VID0	Asynch CMOS	Output
AM3	VID2	Asynch CMOS	Output
AM4	VSS	Power/Other	
AM5	VID6	Asynch CMOS	Output
AM6	FC40	Power/Other	
AM7	VID7	Asynch CMOS	Output
AM8	VCC	Power/Other	
AM9	VCC	Power/Other	
AM20	VSS	Power/Other	
AM21	VCC	Power/Other	
AM22	VCC	Power/Other	
AM23	VSS	Power/Other	
AM24	VSS	Power/Other	

Table 23. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AM25	VCC	Power/Other	
AM26	VCC	Power/Other	
AM27	VSS	Power/Other	
AM28	VSS	Power/Other	
AM29	VCC	Power/Other	
AM30	VCC	Power/Other	
AN1	VSS	Power/Other	
AN2	VSS	Power/Other	
AN3	VCC_SENSE	Power/Other	Output
AN4	VSS_SENSE	Power/Other	Output
AN5	VCC_MB_ REGULATION	Power/Other	Output
AN6	VSS_MB_ REGULATION	Power/Other	Output
AN7	VID_SELECT	Power/Other	Output
AN8	VCC	Power/Other	
AN9	VCC	Power/Other	
AN10	VSS	Power/Other	
AN11	VCC	Power/Other	
AN12	VCC	Power/Other	
AN13	VSS	Power/Other	
AN14	VCC	Power/Other	
AN15	VCC	Power/Other	
AN16	VSS	Power/Other	
AN17	VSS	Power/Other	
AN18	VCC	Power/Other	
AN19	VCC	Power/Other	
AN20	VSS	Power/Other	
AN21	VCC	Power/Other	
AN22	VCC	Power/Other	
AN23	VSS	Power/Other	
AN24	VSS	Power/Other	
AN25	VCC	Power/Other	
AN26	VCC	Power/Other	
AN27	VSS	Power/Other	
AN28	VSS	Power/Other	
AN29	VCC	Power/Other	
AN30	VCC	Power/Other	

4.2 Alphabetical Signals Reference

Table 24. Signal Description (Sheet 1 of 10)

Name	Type	Description
A[35:3]#	Input/ Output	A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these signals transmit the address of a transaction. In sub-phase 2, these signals transmit transaction type information. These signals must connect the appropriate pins/lands of all agents on the processor FSB. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# signals to determine power-on configuration. See Section 6.1 for more details.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/ Output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# signals. All bus agents observe the ADS# activation to begin protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** — **Associated Strobe** REQ[4:0]#, A[16:3]# — ADSTB0# A[35:17]# — ADSTB1#
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the FSB frequency. All processor FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Table 24. Signal Description (Sheet 2 of 10)

Name	Type	Description
BPM[5:0]#	Input/ Output	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins/lands of all processor FSB agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor. These signals do not have on-die termination. Refer to Section 2.6.2 for termination requirements.
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor FSB. It must connect the appropriate pins/lands of all processor FSB agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by de-asserting BPRI#.
BR0#	Input/ Output	BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this signal is sampled to determine the agent ID = 0. This signal does not have on-die termination and must be terminated.
BSEL[2:0]	Output	The BCLK[1:0] frequency select signals BSEL[2:0] are used to select the processor input clock frequency. Table 16 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset, and clock synthesizer. All agents must operate at the same frequency. For more information about these signals, including termination recommendations refer to Section 2.8.2.
COMP[3:0], COMP8	Analog	COMP[3:0] and COMP8 must be terminated to V_{SS} on the system board using precision resistors.

Table 24. Signal Description (Sheet 3 of 10)

Name	Type	Description
D[63:0]#	Input/ Output	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor FSB agents, and must connect the appropriate pins/lands on all such agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will, thus, be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DBI#. Quad-Pumped Signal Groups **Data Group** / **DSTBN# / DSTBP#** / **DBI#** D[15:0]# — 0 — 0 D[31:16]# — 1 — 1 D[47:32]# — 2 — 2 D[63:48]# — 3 — 3 Furthermore, the DBI# signals determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBI[3:0]#	Input/ Output	DBI[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals.The DBI[3:0]# signals are activated when the data on the data bus is inverted. If more than half the data bits, within a 16-bit group, would have been asserted electrically low, the bus agent may invert the data bus signals for that particular sub-phase for that 16-bit group. DBI[3:0] Assignment To Data Bus **Bus Signal** / **Data Bus Signals** DBI3# — D[63:48]# DBI2# — D[47:32]# DBI1# — D[31:16]# DBI0# — D[15:0]#
DBR#	Output	DBR# (Debug Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.
DBSY#	Input/ Output	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor FSB to indicate that the data bus is in use. The data bus is released after DBSY# is de-asserted. This signal must connect the appropriate pins/lands on all processor FSB agents.

Table 24. Signal Description (Sheet 4 of 10)

Name	Type	Description
DEFER#	Input	DEFER# is asserted by an agent to indicate that a transaction cannot be ensured in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or input/ output agent. This signal must connect the appropriate pins/lands of all processor FSB agents.
DPRSTP#	Input	DPRSTP#, when asserted on the platform, causes the processor to transition from the Deep Sleep State to the Deeper Sleep state. To return to the Deep Sleep State, DPRSTP# must be deasserted. Use of the DPRSTP# pin, and corresponding low power state, requires chipset support and may not be available on all platforms. **NOTE:** Some processors may not have the Deeper Sleep State enabled, refer to the Specification Update for specific sku and stepping guidance.
DPSLP#	Input	DPSLP#, when asserted on the platform, causes the processor to transition from the Sleep State to the Deep Sleep state. To return to the Sleep State, DPSLP# must be deasserted. Use of the DPSLP# pin, and corresponding low power state, requires chipset support and may not be available on all platforms. **NOTE:** Some processors may not have the Deep Sleep State enabled, refer to the Specification Update for specific proceswor and stepping guidance.
DRDY#	Input/ Output	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be de-asserted to insert idle clocks. This signal must connect the appropriate pins/lands of all processor FSB agents.
DSTBN[3:0]#	Input/ Output	DSTBN[3:0]# are the data strobes used to latch in D[63:0]#. **Signals** — **Associated Strobe** D[15:0]#, DBI0# — DSTBN0# D[31:16]#, DBI1# — DSTBN1# D[47:32]#, DBI2# — DSTBN2# D[63:48]#, DBI3# — DSTBN3#
DSTBP[3:0]#	Input/ Output	DSTBP[3:0]# are the data strobes used to latch in D[63:0]#. **Signals** — **Associated Strobe** D[15:0]#, DBI0# — DSTBP0# D[31:16]#, DBI1# — DSTBP1# D[47:32]#, DBI2# — DSTBP2# D[63:48]#, DBI3# — DSTBP3#
FC0/BOOTSELECT	Other	FC0/BOOTSELECT is not used by the processor. When this land is tied to Vss previous processors based on the Intel NetBurst® microarchitecture should be disabled and prevented from booting.
FCx	Other	FC signals are signals that are available for compatibility with other processors.

Table 24. Signal Description (Sheet 5 of 10)

Name	Type	Description
FERR#/PBE#	Output	FERR#/PBE# (floating point error/pending break event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. For additional information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to volume 3 of the *Intel Architecture Software Developer's Manual* and the *Intel Processor Identification and the CPUID Instruction* application note.
GTLREF[1:0]	Input	GTLREF[1:0] determine the signal reference level for GTL+ input signals. GTLREF is used by the GTL+ receivers to determine if a signal is a logical 0 or logical 1.
HIT# HITM#	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#. This signal does not have on-die termination. Refer to Section 2.6.2 for termination requirements.
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is de-asserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/ Output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins/lands of all processor FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).

Table 24. Signal Description (Sheet 6 of 10)

Name	Type	Description
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins/lands of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/ INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these signals as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins/lands of all processor FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor FSB, it will wait until it observes LOCK# de-asserted. This enables symmetric agents to retain ownership of the processor FSB throughout the bus locked operation and ensure the atomicity of lock.
MSID[1:0]	Output	On the processor these signals are connected on the package to Vss. As an alternative to MSID, Intel has implemented the Power Segment Identifier (PSID) to report the maximum Thermal Design Power of the processor. Refer to Section 2.5 for additional information regarding PSID.
PECI	Input/ Output	PECI is a proprietary one-wire bus interface. See Chapter 5.3 for details.
PROCHOT#	Input/ Output	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system de-asserts PROCHOT#. See Section 5.2.4 for more details.
PSI#	Output	Processor Power Status Indicator Signal. This signal may be asserted when the processor is in the Deeper Sleep State. PSI# can be used to improve load efficiency of the voltage regulator, resulting in platfrom power savings.

Table 24. Signal Description (Sheet 7 of 10)

Name	Type	Description
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins/lands of all processor FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, all FSB agents will de-assert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 6.1. This signal does not have on-die termination and must be terminated on the system board.
RESERVED		All RESERVED lands must remain unconnected. Connection of these lands to V_{CC}, V_{SS}, V_{TT}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins/lands of all processor FSB agents.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this signal to determine if the processor is present.

Table 24. Signal Description (Sheet 8 of 10)

Name	Type	Description
SLP#	Input	SLP# (Sleep), when asserted in Extended Stop Grant or Stop Grant state, causes the processor to enter the Sleep state. In the Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is de-asserted, the processor exits Sleep state and returns to Extended Stop Grant or Stop Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state. Use of the SLP# pin, and corresponding low power state, requires chipset support and may not be available on all platforms. **NOTE:** Some processors may not have the Sleep State enabled, refer to the Specification Update for specific processor and stepping guidance.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the de-assertion of RESET#, the processor will tri-state its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is de-asserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[12,10:0]	Input	The TESTHI[12,10:0] lands must be connected to the processor's appropriate power source (refer to VTT_OUT_LEFT and VTT_OUT_RIGHT signal description) through a resistor for proper processor operation. See Section 2.4 for more details.

Table 24. Signal Description (Sheet 9 of 10)

Name	Type	Description
THERMTRIP#	Output	In the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature approximately 20 °C above the maximum T_C. Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond where permanent silicon damage may occur. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus, halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (V_{CC}) must be removed following the assertion of THERMTRIP#. Driving of the THERMTRIP# signal is enabled within 10 µs of the assertion of PWRGOOD (provided V_{TT} and V_{CC} are asserted) and is disabled on de-assertion of PWRGOOD (if V_{TT} or V_{CC} are not valid, THERMTRIP# may also be disabled). Once activated, THERMTRIP# remains latched until PWRGOOD, V_{TT} or V_{CC} is de-asserted. While the de-assertion of the PWRGOOD, V_{TT} or V_{CC} signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted within 10 µs of the assertion of PWRGOOD (provided V_{TT} and V_{CC} are valid).
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins/lands of all FSB agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.
VCC	Input	VCC are the power pins for the processor. The voltage supplied to these pins is determined by the VID[7:0] pins.
VCCA	Input	VCCA provides isolated power for internal PLLs on previous generation processors. It may be left as a No-Connect on boards supporting the processor.
VCCIOPLL	Input	VCCIOPLL provides isolated power for internal processor FSB PLLs on previous generation processors. It may be left as a No-Connect on boards supporting the processor.
VCCPLL	Input	VCCPLL provides isolated power for internal processor FSB PLLs.
VCC_SENSE	Output	VCC_SENSE is an isolated low impedance connection to processor core power (V_{CC}). It can be used to sense or measure voltage near the silicon with little noise.
VCC_MB_ REGULATION	Output	This land is provided as a voltage regulator feedback sense point for V_{CC}. It is connected internally in the processor package to the sense point land U27 as described in the *Voltage Regulator Design Guide*.

Table 24. Signal Description (Sheet 10 of 10)

Name	Type	Description
VID[7:0]	Output	The VID (Voltage ID) signals are used to support automatic selection of power supply voltages (V_{CC}). Refer to the *Voltage Regulator Design Guide* for more information. The voltage supply for these signals must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID signals becomes valid. The VID signals are needed to support the processor voltage specification variations. See Table 2 for definitions of these signals. The VR must supply the voltage that is requested by the signals, or disable itself.
VID_SELECT	Output	This land is tied high on the processor package and is used by the VR to choose the proper VID table. Refer to the *Voltage Regulator Design Guide* for more information.
VRDSEL	Input	This input should be left as a no connect in order for the processor to boot. The processor will not boot on legacy platforms where this land is connected to V_{SS}.
VSS	Input	VSS are the ground pins for the processor and should be connected to the system ground plane.
VSSA	Input	VSSA provides isolated ground for internal PLLs on previous generation processors. It may be left as a No-Connect on boards supporting the processor.
VSS_SENSE	Output	VSS_SENSE is an isolated low impedance connection to processor core V_{SS}. It can be used to sense or measure ground near the silicon with little noise.
VSS_MB_ REGULATION	Output	This land is provided as a voltage regulator feedback sense point for V_{SS}. It is connected internally in the processor package to the sense point land V27 as described in the *Voltage Regulator Design Guide.*
VTT		Miscellaneous voltage supply.
VTT_OUT_LEFT VTT_OUT_RIGHT	Output	The VTT_OUT_LEFT and VTT_OUT_RIGHT signals are included to provide a voltage supply for some signals that require termination to V_{TT} on the motherboard.
VTT_SEL	Output	The VTT_SEL signal is used to select the correct V_{TT} voltage level for the processor. This land is connected internally in the package to V_{SS}.

5 Thermal Specifications and Design Considerations

5.1 Processor Thermal Specifications

The processor requires a thermal solution to maintain temperatures within the operating limits as set forth in Section 5.1.1. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor Integrated Heat Spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

For more information on designing a component level thermal solution, refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2).

Note: The boxed processor will ship with a component thermal solution. Refer to Chapter 7 for details on the boxed processor.

5.1.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum case temperature (T_C) specifications when operating at or below the Thermal Design Power (TDP) value listed per frequency in Table 25. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2).

The processor uses a methodology for managing processor temperatures which is intended to support acoustic noise reduction through fan speed control. Selection of the appropriate fan speed is based on the relative temperature data reported by the processor's Platform Environment Control Interface (PECI) bus as described in Section 5.3. If the value reported via PECI is less than $T_{CONTROL}$, then the case temperature is permitted to exceed the Thermal Profile. If the value reported via PECI is greater than or equal to $T_{CONTROL}$, then the processor case temperature must remain at or below the temperature as specified by the thermal profile. The temperature reported over PECI is always a negative value and represents a delta below the onset of thermal control circuit (TCC) activation, as indicated by PROCHOT# (see Section 5.2). Systems that implement fan speed control must be designed to take these conditions in to account. Systems that do not alter the fan speed only need to ensure the case temperature meets the thermal profile specifications.

In order to determine a processor's case temperature specification based on the thermal profile, it is necessary to accurately measure processor power dissipation. Intel has developed a methodology for accurate power measurement that correlates to Intel test temperature and voltage conditions. Refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2) for the details of this methodology.

The case temperature is defined at the geometric top center of the processor. Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) indicated in Table 25 instead of the maximum processor power consumption. The Thermal Monitor feature is designed to protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained periods of time. For more details on the usage of this feature, refer to Section 5.2. **In all cases the Thermal Monitor or Thermal Monitor 2 feature must be enabled for the processor to remain within specification.**

Table 25. Processor Thermal Specifications

Processor Number	Core Frequency (GHz)	Thermal Design Power (W)[3,4]	Extended HALT Power (W)[1]	Deeper Sleep Power (W)[2]	775_VR_CONFIG_06 Guidance[5]	Minimum T_C (°C)	Maximum T_C (°C)	Notes
E5200 E5300	2.50 2.66	65.0 65.0	8 8	6 4	775_VR_CONFIG_06 (65 W)	5 5	See Table 26 and Figure 13	

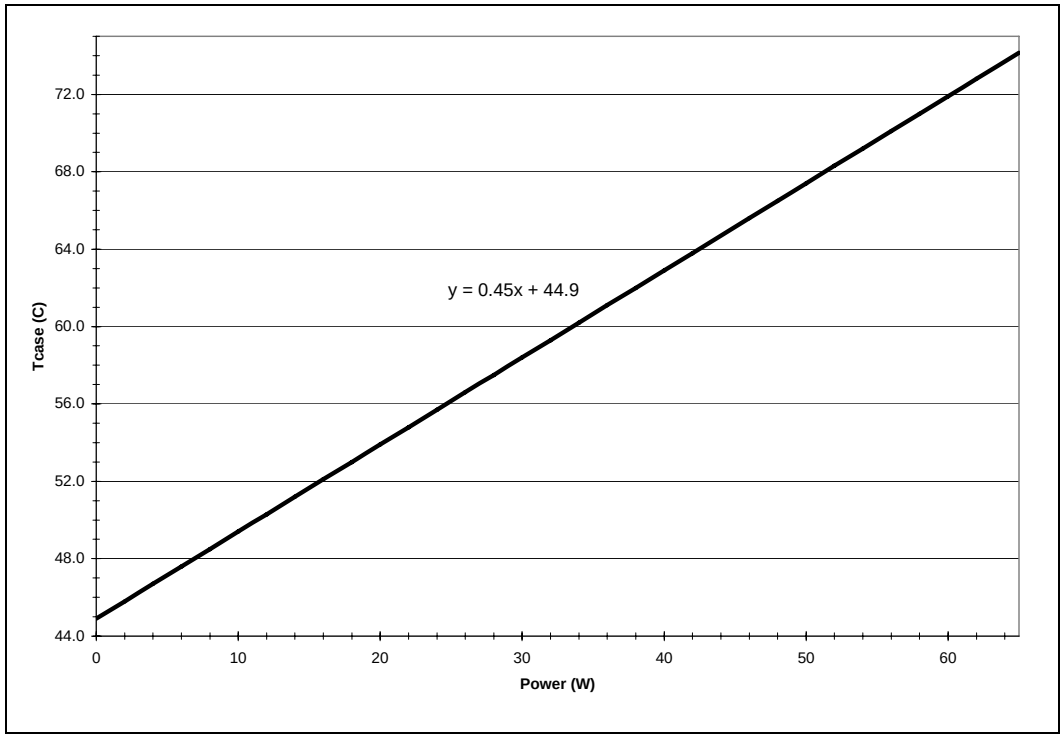
NOTES:

1. Specification is at 36 °C T_C and minimum voltage loadline. Specification is ensured by design characterization and not 100% tested.
2. Specification is at 34 °C T_C and minimum voltage loadline. Specification is ensured by design characterization and not 100% tested.
3. Thermal Design Power (TDP) should be used for processor thermal solution design targets. The TDP is not the maximum power that the processor can dissipate.
4. This table shows the maximum TDP for a given frequency range. Individual processors may have a lower TDP. Therefore, the maximum T_C will vary depending on the TDP of the individual processor. Refer to thermal profile figure and associated table for the allowed combinations of power and T_C.
5. 775_VR_CONFIG_06 guidelines provide a design target for meeting future thermal requirements.

Table 26. Processor Thermal Profile

Power (W)	Maximum Tc (°C)	Power	Maximum Tc (°C)	Power	Maximum Tc (°C)
0	44.9	24	55.7	48	66.5
2	45.8	26	56.6	50	67.4
4	46.7	28	57.5	52	68.3
6	47.6	30	58.4	54	69.2
8	48.5	32	59.3	56	70.1
10	49.4	34	60.2	58	71.0
12	50.3	36	61.1	60	71.9
14	51.2	38	62.0	62	72.8
16	52.1	40	62.9	64	73.7
18	53.0	42	63.8	65	74.1
20	53.9	44	64.7		
22	54.8	46	65.6		

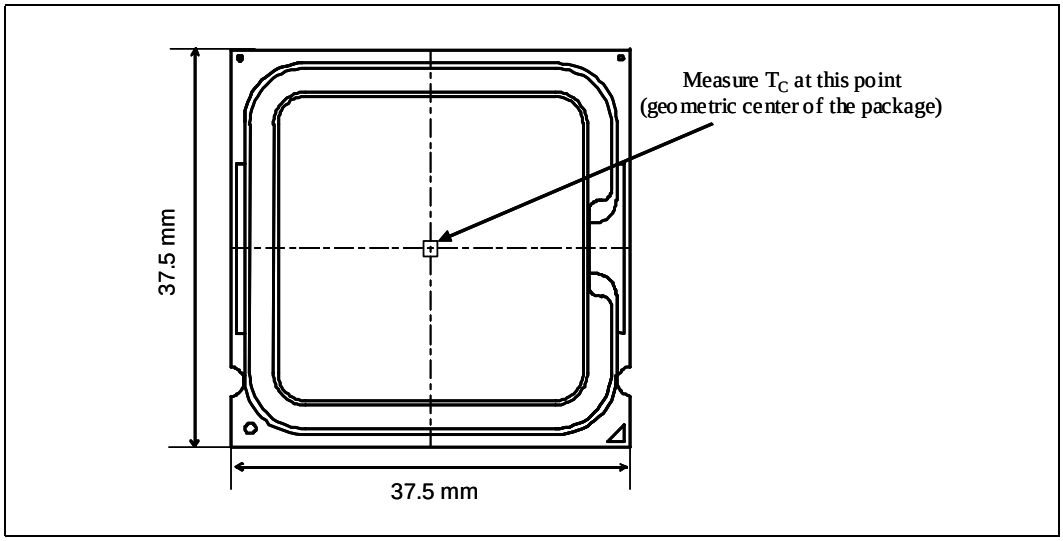
Figure 13. Processor Series Thermal Profile



5.1.2 Thermal Metrology

The maximum and minimum case temperatures (T_C) for the processor is specified in Table 25. This temperature specification is meant to help ensure proper operation of the processor. Figure 14 illustrates where Intel recommends T_C thermal measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2).

Figure 14. Case Temperature (T_C) Measurement Location



5.2 Processor Thermal Features

5.2.1 Thermal Monitor

The Thermal Monitor feature helps control the processor temperature by activating the thermal control circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption by modulating (starting and stopping) the internal processor core clocks. **The Thermal Monitor feature must be enabled for the processor to be operating within specifications.** The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the Thermal Monitor feature is enabled, and a high temperature situation exists (i.e., TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30–50%). Clocks often will not be off for more than 3.0 microseconds when the TCC is active. Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief

periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may result in a T_C that exceeds the specified maximum temperature and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2) for information on designing a thermal solution.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

5.2.2 Thermal Monitor 2

The processor also supports an additional power reduction capability known as Thermal Monitor 2. This mechanism provides an efficient means for limiting the processor temperature by reducing the power consumption within the processor.

When Thermal Monitor 2 is enabled, and a high temperature situation is detected, the Thermal Control Circuit (TCC) will be activated. The TCC causes the processor to adjust its operating frequency (via the bus multiplier) and input voltage (via the VID signals). This combination of reduced frequency and VID results in a reduction to the processor power consumption.

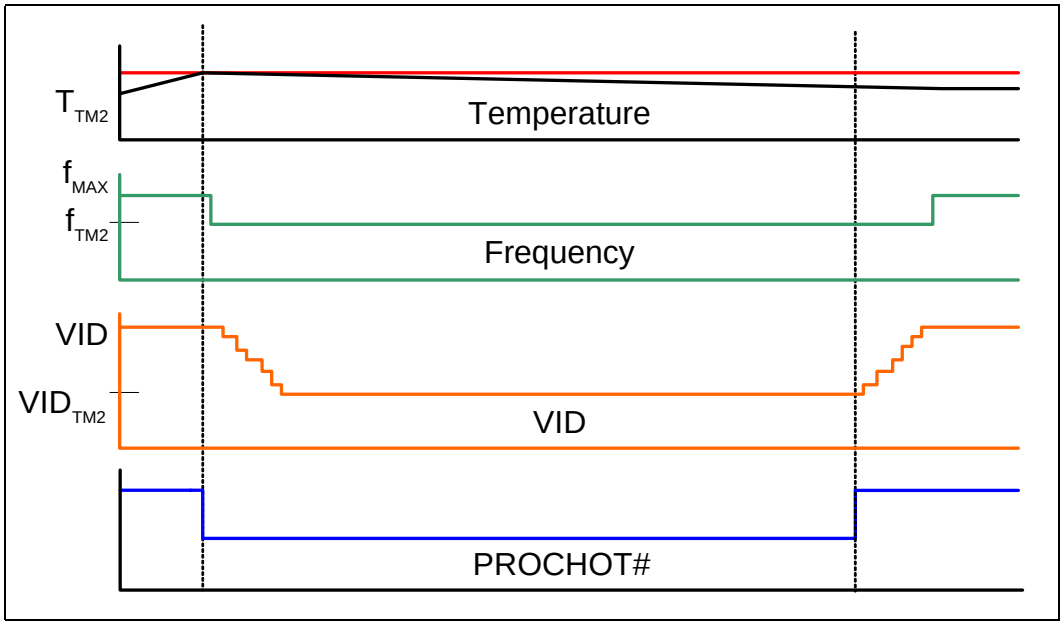
A processor enabled for Thermal Monitor 2 includes two operating points, each consisting of a specific operating frequency and voltage. The first operating point represents the normal operating condition for the processor. Under this condition, the core-frequency-to-FSB multiple used by the processor is that contained in the CLK_GEYSIII_STAT MSR and the VID is that specified in Table 4. These parameters represent normal system operation.

The second operating point consists of both a lower operating frequency and voltage. When the TCC is activated, the processor automatically transitions to the new frequency. This transition occurs very rapidly (on the order of 5 µs). During the frequency transition, the processor is unable to service any bus requests, and consequently, all bus traffic is blocked. Edge-triggered interrupts will be latched and kept pending until the processor resumes operation at the new frequency.

Once the new operating frequency is engaged, the processor will transition to the new core operating voltage by issuing a new VID code to the voltage regulator. The voltage regulator must support dynamic VID steps in order to support Thermal Monitor 2. During the voltage change, it will be necessary to transition through multiple VID codes to reach the target operating voltage. Each step will likely be one VID table entry (see Table 4). The processor continues to execute instructions during the voltage transition. Operation at the lower voltage reduces the power consumption of the processor.

A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the operating frequency and voltage transition back to the normal system operating point. Transition of the VID code will occur first, in order to ensure proper operation once the processor reaches its normal operating frequency. Refer to Figure 15 for an illustration of this ordering.

Figure 15. Thermal Monitor 2 Frequency and Voltage Ordering



The PROCHOT# signal is asserted when a high temperature situation is detected, regardless of whether Thermal Monitor or Thermal Monitor 2 is enabled.

It should be noted that the Thermal Monitor 2 TCC cannot be activated via the on demand mode. The Thermal Monitor TCC, however, can be activated through the use of the on demand mode.

5.2.3 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as “On-Demand” mode and is distinct from the Thermal Monitor feature. On-Demand mode is intended as a means to reduce system level power consumption. Systems using the processor must not rely on software usage of this mechanism to limit the processor temperature.

If bit 4 of the ACPI P_CNT Control Register (located in the processor IA32_THERM_CONTROL MSR) is written to a '1', the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI P_CNT Control Register. In On-Demand mode, the duty cycle can be programmed from 12.5% on/87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used in conjunction with the Thermal Monitor. If the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

5.2.4 PROCHOT# Signal

An external signal, PROCHOT# (processor hot), is asserted when the processor core temperature has reached its maximum operating temperature. If the Thermal Monitor is enabled (note that the Thermal Monitor must be enabled for the processor to be

operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

PROCHOT# is a bi-directional signal. As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that one or both cores has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled, for both cores. The TCC will remain active until the system de-asserts PROCHOT#.

Note: PROCHOT# will not be asserted (as an output) or observed (as an input) when the processor is in the Stop Grant, Sleep, Deep Sleep, and Deeper Sleep low-power states, hence the thermal solution must be designed to ensure the processor remains within specification. If the processor enters one of the above low-power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the low-power state and the processor DTS temperature drops below the thermal trip point.

PROCHOT# allows for some protection of various components from over-temperature situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor (either core) has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its Thermal Design Power. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss. Refer to the Voltage Regulator Design Guide for details on implementing the bi-directional PROCHOT# feature.

5.2.5 THERMTRIP# Signal

Regardless of whether or not Thermal Monitor or Thermal Monitor 2 is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in Table 24). At this point, the FSB signal THERMTRIP# will go active and stay active as described in Table 24. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. If THERMTRIP# is asserted, processor core voltage (V_{CC}) must be removed within the timeframe defined in Table 10.

5.3 Platform Environment Control Interface (PECI)

5.3.1 Introduction

PECI offers an interface for thermal monitoring of Intel processor and chipset components. It uses a single wire, thus alleviating routing congestion issues. PECI uses CRC checking on the host side to ensure reliable transfers between the host and client devices. Also, data transfer speeds across the PECI interface are negotiable within a

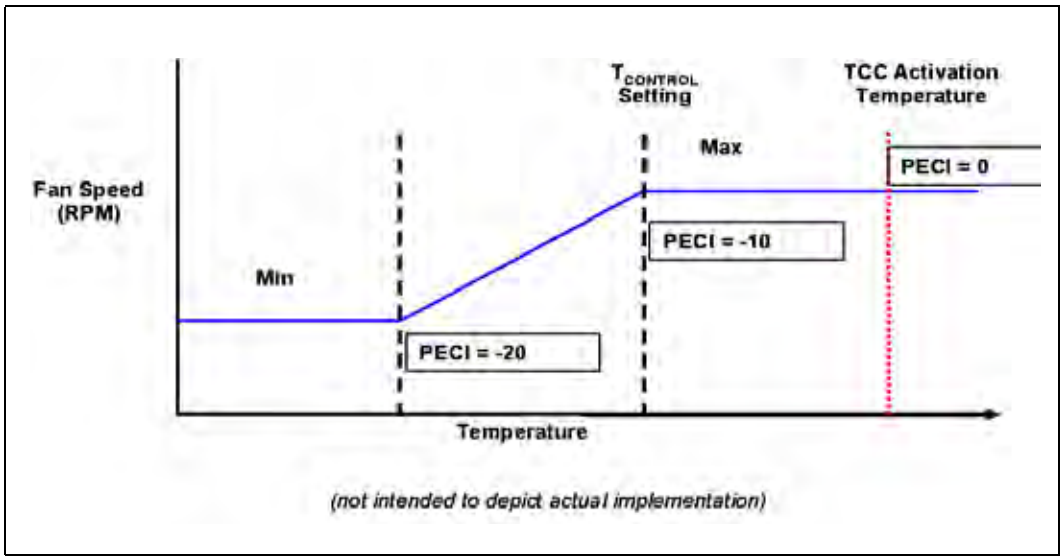
wide range (2 Kbps to 2 Mbps). The PECI interface on the processor is disabled by default and must be enabled through BIOS. More information can be found in the *Platform Environment Control Interface (PECI) Specification*.

5.3.1.1 $T_{CONTROL}$ and TCC activation on PECI-Based Systems

Fan speed control solutions based on PECI utilize a $T_{CONTROL}$ value stored in the processor IA32_TEMPERATURE_TARGET MSR. The $T_{CONTROL}$ MSR uses the same offset temperature format as PECI though it contains no sign bit. Thermal management devices should infer the $T_{CONTROL}$ value as negative. Thermal management algorithms should utilize the relative temperature value delivered over PECI in conjunction with the $T_{CONTROL}$ MSR value to control or optimize fan speeds. Figure 16 shows a conceptual fan control diagram using PECI temperatures.

The relative temperature value reported over PECI represents the delta below the onset of thermal control circuit (TCC) activation as indicated by PROCHOT# assertions. As the temperature approaches TCC activation, the PECI value approaches zero. TCC activates at a PECI count of zero.

Figure 16. Conceptual Fan Control Diagram on PECI-Based Platforms



5.3.2 PECI Specifications

5.3.2.1 PECI Device Address

The PECI register resides at address 30h.

5.3.2.2 PECI Command Support

PECI command support is covered in detail in the *Platform Environment Control Interface Specification*. Refer to this document for details on supported PECI command function and codes.

5.3.2.3 PECI Fault Handling Requirements

PECI is largely a fault tolerant interface, including noise immunity and error checking improvements over other comparable industry standard interfaces. The PECI client is as reliable as the device that it is embedded in, and thus given operating conditions that fall under the specification, the PECI will always respond to requests and the protocol itself can be relied upon to detect any transmission failures. There are, however, certain scenarios where the PECI is know to be unresponsive.

Prior to a power-on RESET# and during RESET# assertion, PECI is not assured to provide reliable thermal data. System designs should implement a default power-on condition that ensures proper processor operation during the time frame when reliable data is not available via PECI.

To protect platforms from potential operational or safety issues due to an abnormal condition on PECI, the Host controller should take action to protect the system from possible damage. It is recommended that the PECI host controller take appropriate action to protect the client processor device if valid temperature readings have not been obtained in response to three consecutive GetTemp()s or for a one second time interval. The host controller may also implement an alert to software in the event of a critical or continuous fault condition.

5.3.2.4 PECI GetTemp0() Error Code Support

The error codes supported for the processor GetTemp() command are listed in Table 27:

Table 27. GetTemp0() Error Codes

Error Code	Description
8000h	General sensor error
8002h	Sensor is operational, but has detected a temperature below its operational range (underflow)

§ §

6 Features

6.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The processor samples the hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifications on these options, refer to Table 28.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor; for configuration purposes, the processor does not distinguish between a "warm" reset and a "power-on" reset.

Table 28. Power-On Configuration Option Signals

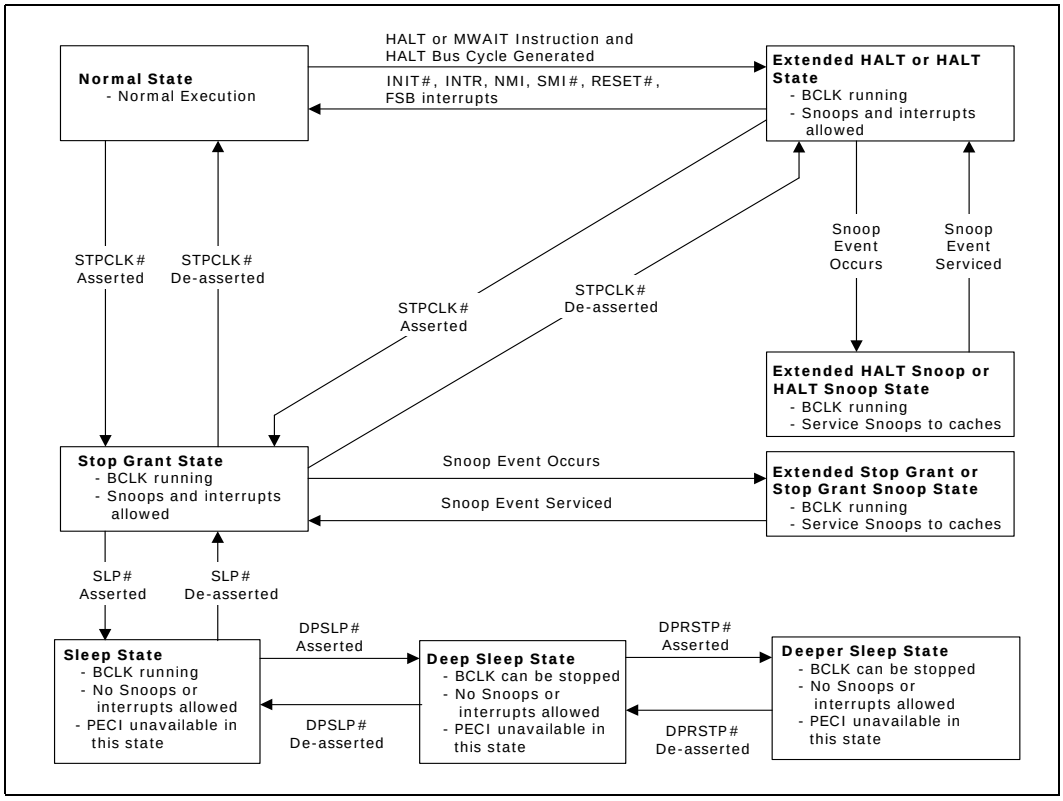
Configuration Option	Signal[1,2]
Output tristate	SMI#
Execute BIST	A3#
Disable dynamic bus parking	A25#
Symmetric agent arbitration ID	BR0#
RESERVED	A[24:4]#, A[35:26]#

NOTE:
1. Asserting this signal during RESET# will select the corresponding option.
2. Address signals not identified in this table as configuration options should not be asserted during RESET#.
3. Disabling of any of the cores within the processors must be handled by configuring the EXT_CONFIG Model Specific Register (MSR). This MSR will allow for the disabling of a single core per die within the processor package.

6.2 Clock Control and Low Power States

The processor allows the use of AutoHALT and Stop-Grant states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 17 for a visual representation of the processor low power states.

Figure 17. Processor Low Power State Machine



6.2.1 Normal State

This is the normal operating state for the processor.

6.2.2 HALT and Extended HALT Powerdown States

The processor supports the HALT or Extended HALT powerdown state. The Extended HALT powerdown state must be configured and enabled via the BIOS for the processor to remain within specification.

The Extended HALT state is a lower power state as compared to the Stop Grant State.

If Extended HALT is not enabled, the default powerdown state entered will be HALT. Refer to the sections below for details about the HALT and Extended HALT states.

6.2.2.1 HALT Powerdown State

HALT is a low power state entered when all the processor cores have executed the HALT or MWAIT instructions. When one of the processor cores executes the HALT instruction, that processor core is halted, however, the other processor continues normal operation. The halted core will transition to the Normal state upon the occurrence of SMI#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the HALT powerdown state. See the *Intel Architecture Software Developer's Manual, Volume 3B: System Programming Guide, Part 2* for more information.

The system can generate a STPCLK# while the processor is in the HALT powerdown state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in HALT powerdown state, the processor will process bus snoops.

6.2.2.2 Extended HALT Powerdown State

Extended HALT is a low power state entered when all processor cores have executed the HALT or MWAIT instructions and Extended HALT has been enabled via the BIOS. When one of the processor cores executes the HALT instruction, that logical processor is halted; however, the other processor continues normal operation. The Extended HALT powerdown state must be enabled via the BIOS for the processor to remain within its specification.

The processor will automatically transition to a lower frequency and voltage operating point before entering the Extended HALT state. Note that the processor FSB frequency is not altered; only the internal core frequency is changed. When entering the low power state, the processor will first switch to the lower bus ratio and then transition to the lower VID.

While in Extended HALT state, the processor will process bus snoops.

The processor exits the Extended HALT state when a break event occurs. When the processor exits the Extended HALT state, it will resume operation at the lower frequency, transition the VID to the original value, and then change the bus ratio back to the original value.

6.2.3 Stop Grant and Extended Stop Grant States

The processor supports the Stop Grant and Extended Stop Grant states. The Extended Stop Grant state is a feature that must be configured and enabled via the BIOS. Refer to the sections below for details about the Stop Grant and Extended Stop Grant states.

6.2.3.1 Stop-Grant State

When the STPCLK# signal is asserted, the Stop Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle.

Since the GTL+ signals receive power from the FSB, these signals should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input signals on the FSB should be driven to the inactive state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal.

A transition to the Grant Snoop state will occur when the processor detects a snoop on the FSB (see Section 6.2.4).

While in the Stop-Grant State, SMI#, INIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process a FSB snoop.

6.2.3.2 Extended Stop Grant State

Extended Stop Grant is a low power state entered when the STPCLK# signal is asserted and Extended Stop Grant has been enabled via the BIOS.

The processor will automatically transition to a lower frequency and voltage operating point before entering the Extended Stop Grant state. When entering the low power state, the processor will first switch to the lower bus ratio and then transition to the lower VID.

The processor exits the Extended Stop Grant state when a break event occurs. When the processor exits the Extended Stop Grant state, it will resume operation at the lower frequency, transition the VID to the original value, and then change the bus ratio back to the original value.

6.2.4 Extended HALT Snoop State, HALT Snoop State, Extended Stop Grant Snoop State, and Stop Grant Snoop State

The Extended HALT Snoop State is used in conjunction with the Extended HALT state. If Extended HALT state is not enabled in the BIOS, the default Snoop State entered will be the HALT Snoop State. Refer to the sections below for details on HALT Snoop State, Stop Grant Snoop State, Extended HALT Snoop State, Extended Stop Grant Snoop State.

6.2.4.1 HALT Snoop State, Stop Grant Snoop State

The processor will respond to snoop transactions on the FSB while in Stop-Grant state or in HALT powerdown state. During a snoop transaction, the processor enters the HALT Snoop State:Stop Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB). After the snoop is serviced, the processor will return to the Stop Grant state or HALT powerdown state, as appropriate.

6.2.4.2 Extended HALT Snoop State, Extended Stop Grant Snoop State

The processor will remain in the lower bus ratio and VID operating point of the Extended HALT state or Extended Stop Grant state.

While in the Extended HALT Snoop State or Extended Stop Grant Snoop State, snoops are handled the same way as in the HALT Snoop State or Stop Grant Snoop State. After the snoop is serviced the processor will return to the Extended HALT state or Extended Stop Grant state.

6.2.5 Sleep State

The Sleep state is a low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and stops all internal clocks. The Sleep state is entered through assertion of the SLP# signal while in the Extended Stop Grant or Stop Grant state. The SLP# pin should only be asserted when the processor is in the Extended Stop Grant or Stop Grant state. SLP# assertions while the processor is not in these states is out of specification and may result in unapproved operation.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP#, DPSLP# or RESET#) are allowed on the FSB while the processor is in Sleep state. Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior. Any transition on an input signal before the processor has returned to the Stop-Grant state will result in unpredictable

behavior.If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through the Stop-Grant state.

If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering an even lower power state, the Deep Sleep state, by asserting the DPSLP# pin (See Section 7.2.6). While the processor is in the Sleep state, the SLP# pin must be deasserted if another asynchronous FSB event needs to occur. PECI is not available and will not respond while in the Sleep State. Refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2) for guidance on how to ensure PECI thermal data is available when the Sleep State is enabled.

6.2.6 Deep Sleep State

The Deep Sleep state is entered through assertion of the DPSLP# pin while in the Sleep state. BCLK may be stopped during the Deep Sleep state for additional platform level power savings. BCLK stop/restart timings on appropriate chipset-based platforms with the CK505 clock chip are as follows:

- **Deep Sleep entry:** the system clock chip may stop/tristate BCLK within two BCLKs of DPSLP# assertion. It is permissible to leave BCLK running during Deep Sleep.
- **Deep Sleep exit:** the system clock chip must drive BCLK to differential DC levels within 2-3 ns of DPSLP# deassertion and start toggling BCLK within 10 BCLK periods.

To re-enter the Sleep state, the DPSLP# pin must be deasserted. BCLK can be restarted after DPSLP# deassertion as described above. A period of 15 microseconds (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin must be deasserted to re-enter the Stop-Grant state.

While in the Deep Sleep state the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions of signals are allowed on the FSB while the processor is in the Deep Sleep state. When the processor is in the Deep Sleep state it will not respond to interrupts or snoop transactions. Any transition on an input signal before the processor has returned to the Stop-Grant state will result in unpredictable behavior. PECI is not available and will not respond while in the Deep Sleep State. Refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2) for guidance on how to ensure PECI thermal data is available when the Deep Sleep State is enabled.

6.2.7 Deeper Sleep State

The Deeper Sleep state is similar to the Deep Sleep state but the core voltage is reduced to a lower level. The Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep state. Exit from Deeper Sleep is initiated by DPRSTP# deassertion. PECI is not available and will not respond while in the Deeper Sleep State. Refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2) for guidance on how to ensure PECI thermal data is available when the Deeper Sleep State is enabled.

In response to entering Deeper Sleep, the processor drives the VID code corresponding to the Deeper Sleep core voltage on the VID pins. Unlike typical Dynamic VID changes (where the steps are single VID steps) the processor will perform a VID jump on the order of 100 mV. To support the Deeper Sleep State the platform must use a VRD 11.1 compliant solution.

6.2.8 Enhanced Intel SpeedStep® Technology

The processor supports Enhanced Intel SpeedStep Technology. This technology enables the processor to switch between frequency and voltage points, which may result in platform power savings. To support this technology, the system must support dynamic VID transitions. Switching between voltage/frequency states is software controlled.

Enhanced Intel SpeedStep Technology is a technology that creates processor performance states (P states). P states are power consumption and capability states within the Normal state as shown in Figure 17. Enhanced Intel SpeedStep Technology enables real-time dynamic switching between frequency and voltage points. It alters the performance of the processor by changing the bus to core frequency ratio and voltage. This allows the processor to run at different core frequencies and voltages to best serve the performance and power requirements of the processor and system. Note that the front side bus is not altered; only the internal core frequency is changed. In order to run at reduced power consumption, the voltage is altered in step with the bus ratio.

The following are key features of Enhanced Intel SpeedStep Technology:

- Voltage/Frequency selection is software controlled by writing to processor MSR's (Model Specific Registers), thus eliminating chipset dependency.
  - If the target frequency is higher than the current frequency, Vcc is incremented in steps (+12.5 mV) by placing a new value on the VID signals after which the processor shifts to the new frequency. Note that the top frequency for the processor can not be exceeded.
  - If the target frequency is lower than the current frequency, the processor shifts to the new frequency and Vcc is then decremented in steps (-12.5 mV) by changing the target VID through the VID signals.

6.3 Processor Power Status Indicator (PSI) Signal

The processor incorporates the PSI# signal that is asserted when the processor is in a reduced power consumption state. PSI# can be used to improve efficiency of the voltage regulator, resulting in platform power savings.

PSI# may be asserted only when the processor is in the Deeper Sleep state.

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7 Boxed Processor Specifications

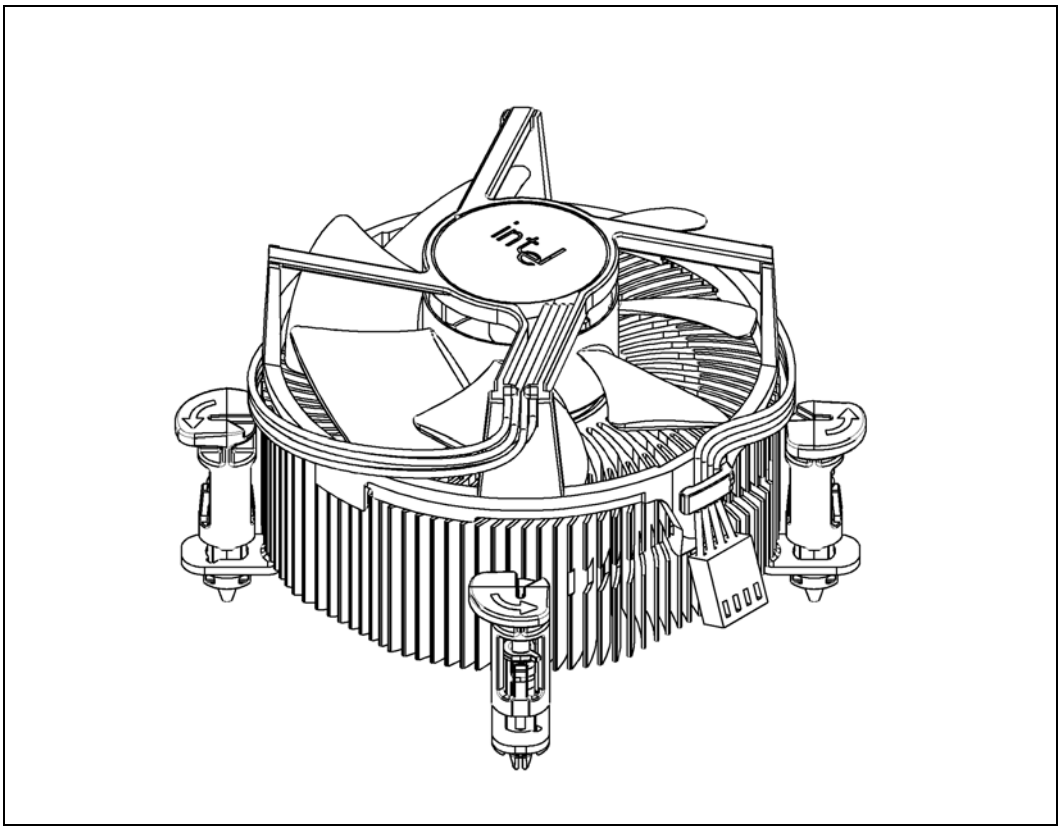
7.1 Introduction

The processor will also be offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from baseboards and standard components. The boxed processor will be supplied with a cooling solution. This chapter documents baseboard and system requirements for the cooling solution that will be supplied with the boxed processor. This chapter is particularly important for OEMs that manufacture baseboards for system integrators.

Note: Unless otherwise noted, all figures in this chapter are dimensioned in millimeters and inches [in brackets]. Figure 18 shows a mechanical representation of a boxed processor.

Note: Drawings in this section reflect only the specifications on the Intel boxed processor product. These dimensions should not be used as a generic keep-out zone for all cooling solutions. It is the system designers' responsibility to consider their proprietary cooling solution when designing to the required keep-out zone on their system platforms and chassis. Refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2*)* for further guidance. Contact your local Intel Sales Representative for this document.

Figure 18. Mechanical Representation of the Boxed Processor



NOTE: The airflow of the fan heatsink is into the center and out of the sides of the fan heatsink.

7.2 Mechanical Specifications

7.2.1 Boxed Processor Cooling Solution Dimensions

This section documents the mechanical specifications of the boxed processor. The boxed processor will be shipped with an unattached fan heatsink. Figure 18 shows a mechanical representation of the boxed processor.

Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the boxed processor with assembled fan heatsink are shown in Figure 19 (Side View), and Figure 20 (Top View). The airspace requirements for the boxed processor fan heatsink must also be incorporated into new baseboard and system designs. Airspace requirements are shown in Figure 24 and Figure 25. Note that some figures have centerlines shown (marked with alphabetic designations) to clarify relative dimensioning.

Figure 19. Space Requirements for the Boxed Processor (Side View)

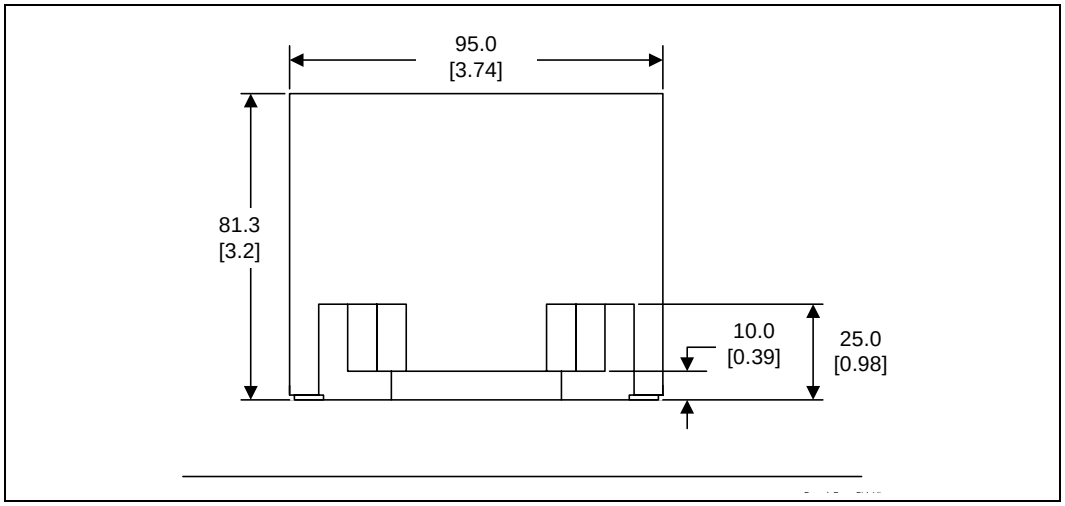
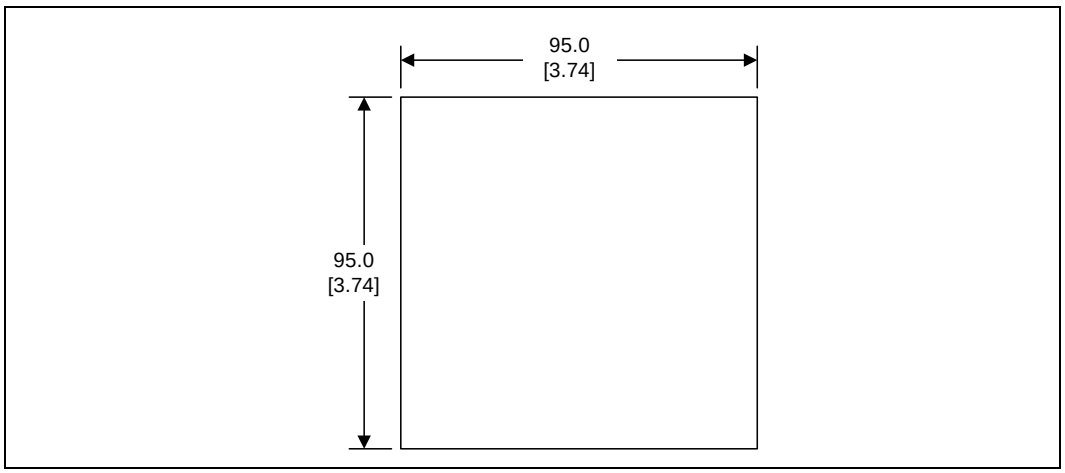


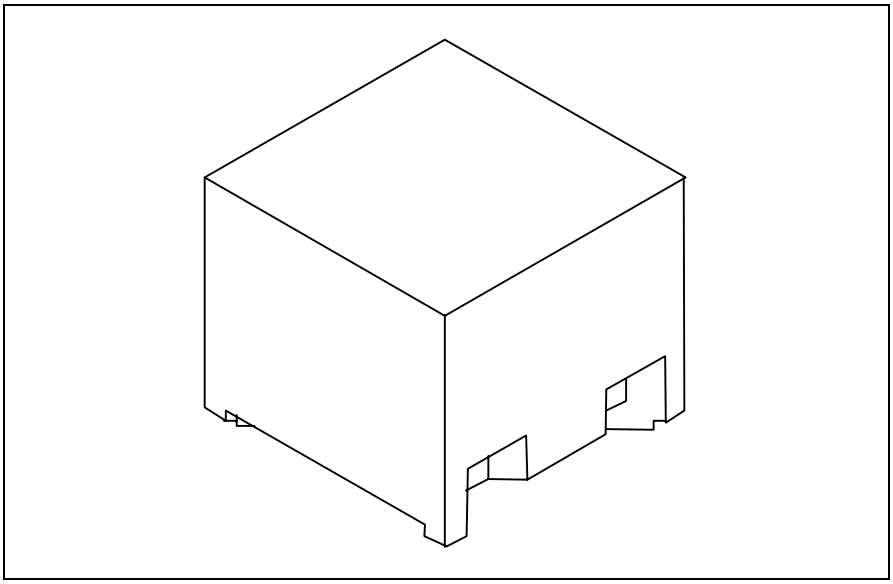
Figure 20. Space Requirements for the Boxed Processor (Top View)



NOTES:

1. Diagram does not show the attached hardware for the clip design and is provided only as a mechanical representation.

Figure 21. Overall View Space Requirements for the Boxed Processor



7.2.2 Boxed Processor Fan Heatsink Weight

The boxed processor fan heatsink will not weigh more than 450 grams. See Chapter 5 and the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2) for details on the processor weight and heatsink requirements.

7.2.3 Boxed Processor Retention Mechanism and Heatsink Attach Clip Assembly

The boxed processor thermal solution requires a heatsink attach clip assembly, to secure the processor and fan heatsink in the baseboard socket. The boxed processor will ship with the heatsink attach clip assembly.

7.3 Electrical Requirements

7.3.1 Fan Heatsink Power Supply

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable will be shipped with the boxed processor to draw power from a power header on the baseboard. The power cable connector and pinout are shown in Figure 22. Baseboards must provide a matched power header to support the boxed processor. Table 29 contains specifications for the input and output signals at the fan heatsink connector.

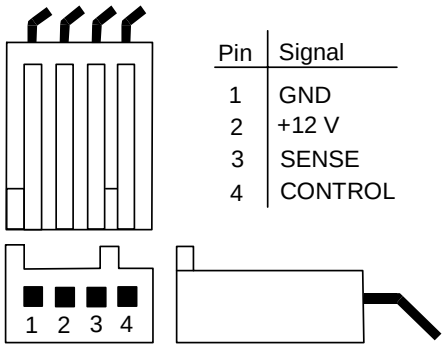
The fan heatsink outputs a SENSE signal, which is an open- collector output that pulses at a rate of 2 pulses per fan revolution. A baseboard pull-up resistor provides V_{OH} to match the system board-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The fan heatsink receives a PWM signal from the motherboard from the 4th pin of the connector labeled as CONTROL.

The boxed processor's fanheat sink requires a constant +12 V supplied to pin 2 and does not support variable voltage control or 3-pin PWM control.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the platform documentation, or on the system board itself. Figure 23 shows the location of the fan power connector relative to the processor socket. The baseboard power header should be positioned within 110 mm [4.33 inches] from the center of the processor socket.

Figure 22. Boxed Processor Fan Heatsink Power Cable Connector Description



Straight square pin, 4-pin terminal housing with polarizing ribs and friction locking ramp.

0.100" pitch, 0.025" square pin width.

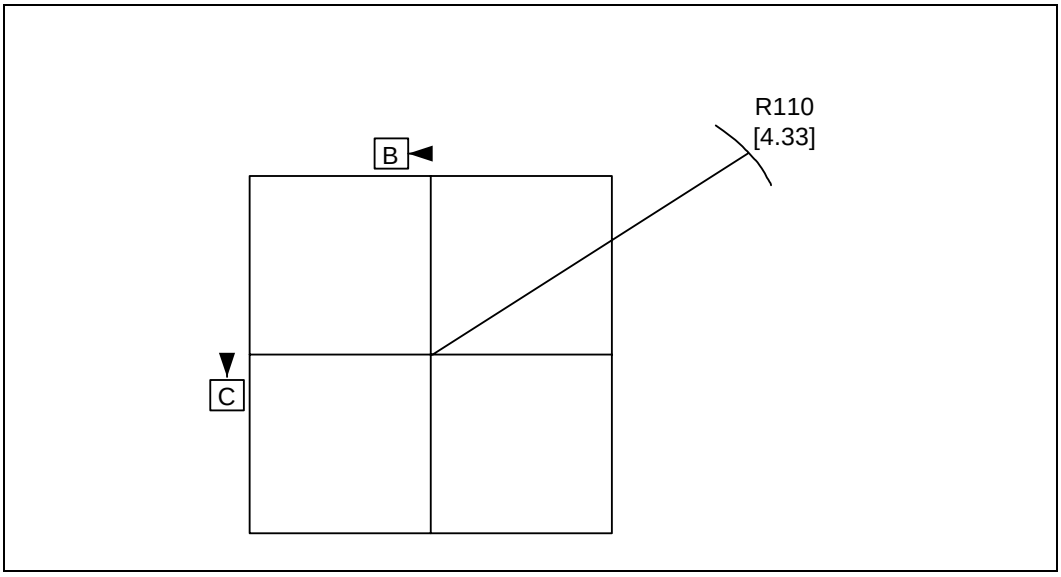
Match with straight pin, friction lock header on mainboard.

Table 29. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max	Unit	Notes
+12 V: 12 volt fan power supply	11.4	12	12.6	V	-
IC:					
• Maximum fan steady-state current draw	—	1.2	—	A	-
• Average fan steady-state current draw	—	0.5	—	A	
• Maximum fan start-up current draw	—	2.2	—	A	
• Fan start-up current draw maximum duration	—	1.0	—	Second	
SENSE: SENSE frequency	—	2	—	pulses per fan revolution	1
CONTROL	21	25	28	kHz	2, 3

NOTES:
1. Baseboard should pull this pin up to 5 V with a resistor.
2. Open drain type, pulse width modulated.
3. Fan will have pull-up resistor for this signal to maximum of 5.25 V.

Figure 23. Baseboard Power Header Placement Relative to Processor Socket



7.4 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution used by the boxed processor.

7.4.1 Boxed Processor Cooling Requirements

The boxed processor may be directly cooled with a fan heatsink. However, meeting the processor's temperature specification is also a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specification is provided in Chapter 5. The boxed processor fan heatsink is able to keep the processor temperature within the specifications (see Table 25) in chassis that provide good thermal management. For the boxed processor fan heatsink to operate properly, it is critical that the airflow provided to the fan heatsink is unimpeded. Airflow of the fan heatsink is into the center and out of the sides of the fan heatsink. Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 24 and Figure 25 illustrate an acceptable airspace clearance for the fan heatsink. The air temperature entering the fan should be kept below 38 ºC. Again, meeting the processor's temperature specification is the responsibility of the system integrator.

Figure 24. Boxed Processor Fan Heatsink Airspace Keepout Requirements (side 1 view)

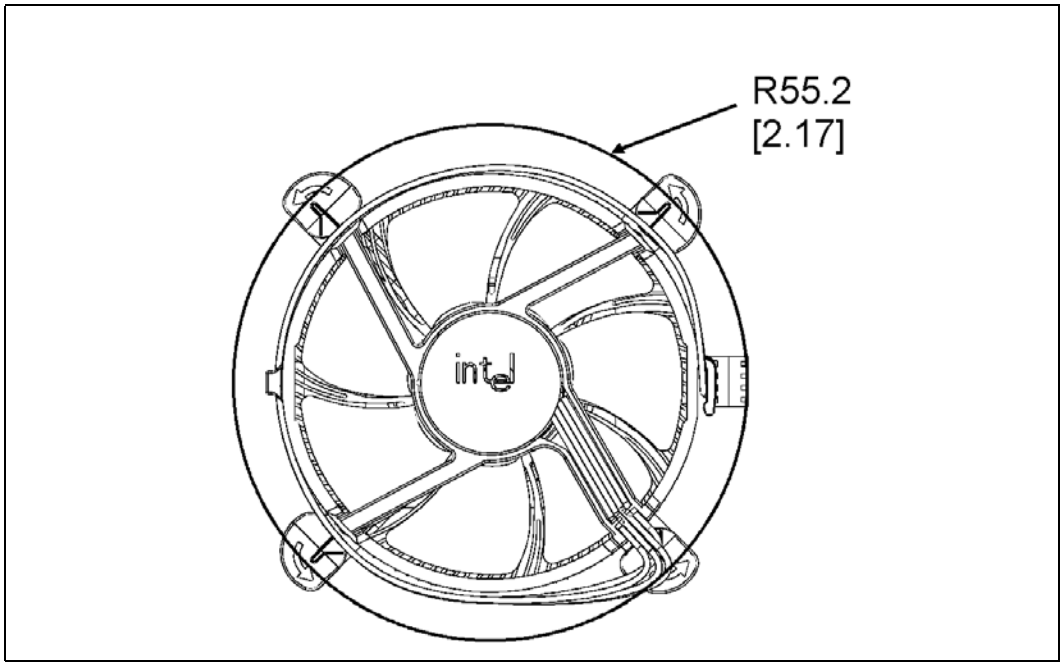
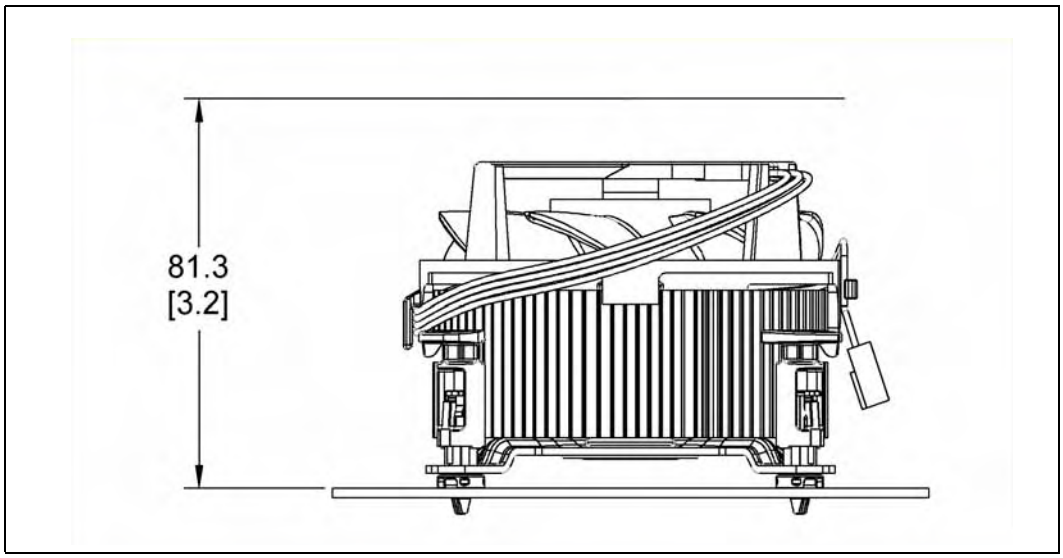


Figure 25. Boxed Processor Fan Heatsink Airspace Keepout Requirements (side 2 view)



7.4.2 Variable Speed Fan

If the boxed processor fan heatsink 4-pin connector is connected to a 3-pin motherboard header it will operate as follows:

The boxed processor fan will operate at different speeds over a short range of internal chassis temperatures. This allows the processor fan to operate at a lower speed and noise level, while internal chassis temperatures are low. If internal chassis temperature increases beyond a lower set point, the fan speed will rise linearly with the internal temperature until the higher set point is reached. At that point, the fan speed is at its maximum. As fan speed increases, so does fan noise levels. Systems should be designed to provide adequate air around the boxed processor fan heatsink that remains cooler then lower set point. These set points, represented in Figure 26 and Table 30, can vary by a few degrees from fan heatsink to fan heatsink. The internal chassis temperature should be kept below 38 ºC. Meeting the processor's temperature specification (see Chapter 5) is the responsibility of the system integrator.

The motherboard must supply a constant +12 V to the processor's power header to ensure proper operation of the variable speed fan for the boxed processor. Refer to Table 29 for the specific requirements.

Figure 26. Boxed Processor Fan Heatsink Set Points

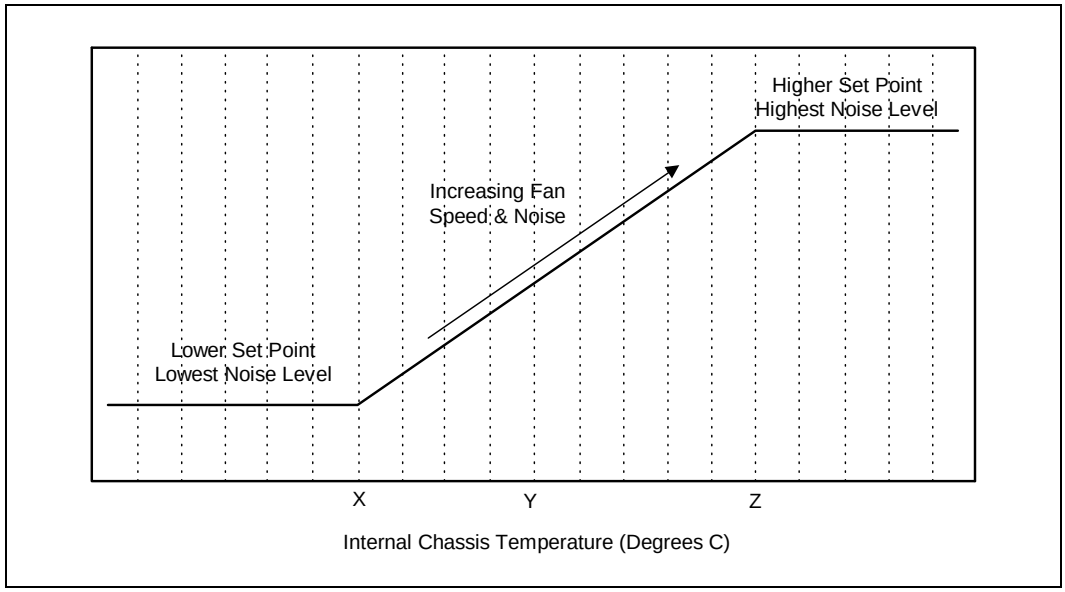


Table 30. Fan Heatsink Power and Signal Specifications

Boxed Processor Fan Heatsink Set Point (°C)	Boxed Processor Fan Speed	Notes
X ≤ 30	When the internal chassis temperature is below or equal to this set point, the fan operates at its lowest speed. Recommended maximum internal chassis temperature for nominal operating environment.	1
Y = 35	When the internal chassis temperature is at this point, the fan operates between its lowest and highest speeds. Recommended maximum internal chassis temperature for worst-case operating environment.	-
Z ≥ 38	When the internal chassis temperature is above or equal to this set point, the fan operates at its highest speed.	-

NOTES:
1. Set point variance is approximately ± 1 °C from fan heatsink to fan heatsink.

If the boxed processor fan heatsink 4-pin connector is connected to a 4-pin motherboard header and the motherboard is designed with a fan speed controller with PWM output (CONTROL see Table 29) and remote thermal diode measurement capability the boxed processor will operate as follows:

As processor power has increased the required thermal solutions have generated increasingly more noise. Intel has added an option to the boxed processor that allows system integrators to have a quieter system in the most common usage.

The 4th wire PWM solution provides better control over chassis acoustics. This is achieved by more accurate measurement of processor die temperature through the processor's Digital Thermal Sensors (DTS) and PECI. Fan RPM is modulated through the use of an ASIC located on the motherboard that sends out a PWM control signal to the 4th pin of the connector labeled as CONTROL. The fan speed is based on actual processor temperature instead of internal ambient chassis temperatures.

If the new 4-pin active fan heat sink solution is connected to an older 3-pin baseboard processor fan header, it will default back to a thermistor controlled mode, allowing compatibility with existing 3-pin baseboard designs. Under thermistor controlled mode, the fan RPM is automatically varied based on the Tinlet temperature measured by a thermistor located at the fan inlet.

For more details on specific motherboard requirements for 4-wire based fan speed control, refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2).

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8 Debug Tools Specifications

8.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Intel Pentium® dual-core processor E5000 series systems. Tektronix and Agilent should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Intel Pentium® dual-core processor E5000 series systems, the LAI is critical in providing the ability to probe and capture FSB signals. There are two sets of considerations to keep in mind when designing an Intel Pentium® dual-core processor E5000 series system that can make use of an LAI: mechanical and electrical.

8.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI lands plug into the processor socket, while the processor lands plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may differ from the space normally occupied by the processor heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

8.1.2 Electrical Considerations

The LAI will also affect the electrical performance of the FSB; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution it provides.

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